REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate paragraphs to current requirements. – RDC	25-03-19	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** https://www.dla.mil/landandmaritime
Original date of drawing YY MM DD 19-05-17	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR-DIGITAL, PROCESSOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/15602**
	REV **A**	**PAGE** 1 **OF** 136

AMSC N/A

5962-V055-25

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Processor microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/15602	-	01	X	F
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AM3558 –EP	Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	324	Plastic Ball Grid Array 1/

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of Sn = 63%, Pb = 34.5, Ag = 2% and Sb = 0.5 %.

1.3 Absolute maximum ratings. 1/ 2/

Over junction temperature range (unless otherwise noted)

		Min	Max	Unit
VDD_MPU	Supply voltage for the MPU core domain	-0.5	1.5	V
VDD_CORE	Supply voltage for the core domain	-0.5	1.5	V
CAP_VDD_RTC 3/	Supply voltage for the RTC core domain	-0.5	1.5	V
VPP 4/	Supply voltage for the RTC domain	-0.5	2.2	V
VDDS_RTC	Supply voltage for the RTC domain	-0.5	2.1	V
VDDS_OSC	Supply voltage for the System oscillator	-0.5	2.1	V
VDDS_SRAM_CORE_BG	Supply voltage for the Core SRAM LDOs	-0.5	2.1	V
VDDS_SRAM_MPU_BB	Supply voltage for the MPU SRAM LDOs	-0.5	2.1	V
VDDS_PLL_DDR	Supply voltage for the DPLL DDR	-0.5	2.1	V
VDDS_PLL_CORE_LCD	Supply voltage for the DPLL Core and LCD	-0.5	2.1	V
VDDS_PLL_MPU	Supply voltage for the DPLL MPU	-0.5	2.1	V
VDDS_DDR	Supply voltage for the DDR IO domain	-0.5	2.1	V
VDDS	Supply voltage for all dual-voltage IO domains	-0.5	2.1	V
VDDA1P8V_USB0	Supply voltage for USBPHY	-0.5	2.1	V
VDDA1P8V_USB1	Supply voltage for USBPHY	-0.5	2.1	V
VDDA_ADC	Supply voltage for ADC	-0.5	2.1	V
VDDSHV1	Supply voltage for the dual-voltage IO domain	-0.5	3.8	V
VDDSHV2	Supply voltage for the dual-voltage IO domain	-0.5	3.8	V
VDDSHV3	Supply voltage for the dual-voltage IO domain	-0.5	3.8	V
VDDSHV4	Supply voltage for the dual-voltage IO domain	-0.5	3.8	V
VDDSHV5	Supply voltage for the dual-voltage IO domain	-0.5	3.8	V
VDDSHV6	Supply voltage for the dual-voltage IO domain	-0.5	3.8	V
VDDA3P3V_USB0	Supply voltage for USBPHY	-0.5	4	V
VDDA3P3V_USB1	Supply voltage for USBPHY	-0.5	4	V
USB0_VBUS 5/	Supply voltage for USB VBUS comparator input	-0.5	5.25	V
USB1_VBUS 5/	Supply voltage for USB VBUS comparator input	-0.5	5.25	V
DDR_VREF	Supply voltage for the DDR SSTL and HSTL reference voltage	-0.5	1.1	V
Steady state max voltage at all IO pins 6/		-0.5 V to IO supply voltage +0.3 V		
USB0_ID 7/	Steady state maximum voltage for the USB ID input	-0.5	2.1	V
USB1_ID 7/	Steady state maximum voltage for the USB ID input	-0.5	2.1	V
Transient overshoot and undershoot specification at IO terminal		25% of corresponding IO supply voltage for up to 30% of signal period		
Latch-up performance 8/	Class II (105°C)	45		mA
Junction temperature, TJ		-40	125	°C
Storage temperature, Tstg 9/		-55	155	°C

1.4 ESD ratings.

Electrostatic discharge (ESD) performance (VESD):
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001 ..... ±2000 V 10/
Charged Device Model (CDM), per JESD22-C101 ..... ±500 V 11/

1.5 Power-On Hours (POH).

Reliability Data 12/ 13/ 14/ 15/

Operating Condition	EXTENDED	
	Junction Temp (T_J)	Lifetime (POH) 16/
Turbo	–40°C to 105°C	80K
OPP120	–40°C to 105°C	100K
OPP100	–40°C to 105°C	100K
OPP50	–40°C to 105°C	100K

1/ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to their associated VSS or VSSA_x.
3/ This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.
4/ During functional operation, this pin is a no connect.
5/ This terminal is connected to a fail-safe IO and does not have a dependence on any IO supply voltage.
6/ This parameter applies to all IO terminals which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.5 to +0.3 V. Apply special attention anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
7/ This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
8/ Based on JEDEC JESD78D [*IC Latch-Up Test*].
9/ For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.
10/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
11/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
12/ The power-on hours (POH) information in this table is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
13/ To avoid significant degradation, the device power-on hours (POH) must be limited as described in this table.
14/ Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.
15/ The above notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products
16/ POH = Power-on hours when the device is fully functional.

1.6 Operating Performance Points (OPPs).

VDD_CORE OPPs for Case X Package 17/

VDD_CORE OPP Device Rev. "Blank"	VDD_CORE			DDR3 18 DDR3L	DDR2 18/	mDDR 18/	L3 and L4
	Min	NOM	Max				
OPP100	1.056 V	1.100 V	1.144 V	400 MHz	266 MHz	200 MHz	200 and 100 MHz
OPP50	0.912 V	0.950 V	0.998 V		125 MHz	90 MHz	100 and 50 MHz

Valid Combinations of VDD_CORE and VDD_MPU OPPs for case X Package 17/ 18/

VDD_CORE	VDD_MPU
OPP50	OPP100
OPP100	OPP100
OPP100	OPP120
OPP100	Turbo

VDD_MPU OPPs for Case X Package 17/

VDD_MPU OPP	VDD_MPU			ARM (A8)
	Min	NOM	Max	
Turbo	1.210 V	1.260 V	1.326 V	800 MHz
OPP120	1,152 V	1.200 V	1.248 V	720 MHz
OPP100	1.056 V	1.100 V	1.144 V	600 MHz
OPP100	0.912 V	0.950 V	0.988 V	300 MHz

Valid Combinations of VDD_CORE and VDD_MPU OPPs for case X Package

VDD_CORE	VDD_MPU
OPP50	OPP50
OPP50	OPP100
OPP100	OPP50
OPP100	OPP100
OPP100	OPP120
OPP100	Turbo

17/ Frequencies in this table indicate maximum performance for a given OPP condition.
18/ This parameter represents the maximum memory clock frequency. Since data is transferred on both edges of the clock, double data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

1.7 Recommended operating conditions.

Over junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	Min	NOM	Max	Unit
VDD_CORE 19/	Supply voltage range for core domain; OPP100	1.056	1.100	1.144	V
	Supply voltage range for core domain; OPP50	0.912	0.950	0.988	
VDD_MPU 19/	Supply voltage range for MPU domain; Turbo	1.210	1.260	1.326	V
	Supply voltage range for MPU domain; OPP120	1.152	1.200	1.248	
	Supply voltage range for MPU domain; OPP100	1.056	1.100	1.144	
	Supply voltage range for MPU domain; OPP50	0.912	0.950	0.988	
CAP_VDD_RTC 20/	Supply voltage range for RTC domain input	0.900	1.100	1.250	V
VDDS_RTC	Supply voltage range for RTC domain	1.710	1.800	1.890	V
VDDS_DDR	Supply voltage range for DDR IO domain (DDR2)	1.710	1.800	1.890	V
	Supply voltage range for DDR IO domain (DDR3)	1.425	1.500	1.575	
	Supply voltage range for DDR IO domain (DDR3L)	1.283	1.350	1.418	
VDDS 21/	Supply voltage range for all dual-voltage IO domains	1.710	1.800	1.890	V
VDDS_SRAM_CORE_BG	Supply voltage range for Core SRAM LDOs, analog	1.710	1.800	1.890	V
VDDS_SRAM_MPU_BB	Supply voltage range for MPU SRAM LDOs, analog	1.710	1.800	1.890	V
VDDS_PLL_DDR 22/	Supply voltage range for DPLL DDR, analog	1.710	1.800	1.890	V
VDDS_PLL_CORE_LCD 22/	Supply voltage range for DPLL CORE and LCD, analog	1.710	1.800	1.890	V
VDDS_PLL_MPU 22/	Supply voltage range for DPLL MPU, analog	1.710	1.800	1.890	V
VDDS_OSC	Supply voltage range for system oscillator IO's, analog	1.710	1.800	1.890	V
VDDA1P8V_USB0 22/	Supply voltage range for USBPHY and PER DPLL analog, 1.8 V	1.710	1.800	1.890	V
VDDA1P8V_USB1	Supply voltage range for USB PHY, analog, 1.8 V	1.710	1.800	1.890	V
VDDA3P3V_USB0	Supply voltage range for USB PHY, analog, 3.3 V	3.135	3.300	3.465	V
VDDA3P3V_USB1	Supply voltage range for USB PHY, analog, 3.3 V	3.135	3.300	3.465	V
VDDA_ADC	Supply voltage range for ADC, analog	1.710	1.800	1.890	V
VDDSHV1	Supply voltage range for dual-voltage IO domain (1.8-V operation)	1.710	1.800	1.890	V
VDDSHV2		1.710	1.800	1.890	V
VDDSHV3		1.710	1.800	1.890	V
VDDSHV4		1.710	1.800	1.890	V
VDDSHV5		1.710	1.800	1.890	V
VDDSHV6		1.710	1.800	1.890	V
VDDSHV1	Supply voltage range for dual-voltage IO domain (3.3-V operation)	3.135	3.300	3.465	V
VDDSHV2		3.135	3.300	3.465	V

See foot notes at end of table.

1.7 Recommended operating conditions- Continued.

Over junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	Min	NOM	Max	Unit
VDDSHV3	Supply voltage range for dual-voltage IO domain (3.3 -V operation)	3.135	3.300	3.465	V
VDDSHV4		3.135	3.300	3.465	V
VDDSHV5		3.135	3.300	3.465	V
VDDSHV6		3.135	3.300	3.465	V
DDR_VREF	Voltage range for DDR SSTL and HSTL reference input (DDR2, DDR3, DDR3L)	0.49 × VDDS_DDR	0.49 × VDDS_DDR	0.49 × VDDS_DDR	V
USB0_VBUS	Voltage range for USB VBUS comparator input	0.000	5.000	5.250	V
USB1_VBUS		0.000	5.000	5.250	V
USB0_ID	Voltage range for the USB ID input	23/			V
USB1_ID		23/			V
Operating temperature range, T_J	Extended temperature	-40		105	°C

1.8 Thermal characteristics.

Thermal metric 3/	Case outline X **(°C/W)** 24/ 25/	**AIR FLOW (m/s)** 26/
Junction to case, $R_{\theta JC}$	10.2	N/A
Junction to board, $R_{\theta JB}$	12.1	N/A
Junction to free air, RΘJA	24.2	0
	20.1	1.0
	19.3	2.0
	18.8	3.0
Junction-to-package top, φ_{JT}	0.3	0.0
	0.6	1.0
	0.7	2.0
	0.8	3.0
Junction-to-board, φ_{JB}	12.7	0.0
	12.3	1.0
	12.3	2.0
	12.2	3.0

19/ The supply voltage defined by OPP100 should be applied to this power domain before the device is released from reset.
20/ This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.
21/ VDDS should be supplied irrespective of 1.8- or 3.3-V mode of operation of the dual-voltage IOs.
22/ For more details on power supply requirements, see Section 6.1.4 from manufacturer data.
23/ This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
24/ These values are based on a JEDEC-defined 2S2P system (with the exception of the theta JC [$R_{\Theta JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:JESD51-2, JESD51-3, JESD51-7, JESD51-9,
25/ °C/W = degrees Celsius per watt.
26/ m/s = meters per second.

1.9 **Power Consumption Summary.**

Maximum Current Ratings at Power Terminals 27/

SUPPLY NAME	DESCRIPTION		Max	Unit
VDD_CORE	Maximum current rating for the core domain; OPP100		400	mA
	Maximum current rating for the core domain; OPP50		250	
VDD_MPU	Maximum current rating for the MPU domain; Turbo	at 800 MHz	800	
	Maximum current rating for the MPU domain; OPP120	at 720 MHz	720	
	Maximum current rating for the MPU domain; OPP100	at 600 MHz	600	
	Maximum current rating for the MPU domain; OPP50	at 400 MHz	300	
CAP_VDD_RTC 28/	Maximum current rating for RTC domain input and LDO output		2	
VDDS_RTC	Maximum current rating for the RTC domain		5	
VDDS_DDR	Maximum current rating for DDR IO domain		250	
VDDS	Maximum current rating for all dual-voltage IO domains		50	
VDDS_SRAM_CORE_BG	Maximum current rating for core SRAM LDOs		10	
VDDS_SRAM_MPU_BB	Maximum current rating for MPU SRAM LDOs		10	
VDDS_PLL_DDR	Maximum current rating for the DPLL DDR		10	
VDDS_PLL_CORE_LCD	Maximum current rating for the DPLL Core and LCD		20	
VDDS_PLL_MPU	Maximum current rating for the DPLL MPU		10	
VDDS_OSC	Maximum current rating for the system oscillator IOs		5	
VDDA1P8V_USB0	Maximum current rating for USBPHY 1.8 V		25	
VDDA1P8V_USB1	Maximum current rating for USBPHY 1.8 V		25	
VDDA3P3V_USB0	Maximum current rating for USBPHY 3.3 V		40	
VDDA3P3V_USB1	Maximum current rating for USBPHY 3.3 V		40	
VDDA_ADC	Maximum current rating for ADC		10	
VDDSHV1	Maximum current rating for dual-voltage IO domain		50	
VDDSHV2	Maximum current rating for dual-voltage IO domain		50	
VDDSHV3	Maximum current rating for dual-voltage IO domain		50	
VDDSHV4	Maximum current rating for dual-voltage IO domain		50	
VDDSHV5	Maximum current rating for dual-voltage IO domain		50	
VDDSHV6	Maximum current rating for dual-voltage IO domain		100	

27/ Current ratings specified in this table are worst-case estimates. Actual application power supply estimates could be lower. For more information, see the manufacturer *AM335x Power Consumption Summary* application report (SPRABN5) on manufacturer data.

28/ This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.

1.9 **Power Consumption Summary- Continued.**

Low-Power Modes Power Consumption Summary

POWER MODES	APPLICATION STATE	POWER DOMAINS, CLOCKS, AND VOLTAGE SUPPLY STATES	NOM	Max	Unit
Standby	DDR memory is in self-refresh and contents are preserved. Wake up from any GPIO. Cortex-A8 context/register contents are lost and must be saved before entering standby. On exit, context must be restored from DDR. For wake-up, boot ROM executes and branches to system resume.	Power supplies: • All power supplies are ON. • VDD_MPU = 0.95 V (nom) • VDD_CORE = 0.95 V (nom) Clocks: • Main Oscillator (OSC0) = ON • All DPLLs are in bypass. Power domains: • PD_PER = ON • PD_MPU = OFF • PD_GFX = OFF • PD_WKUP = ON DDR is in self-refresh.	16.5	22.0	mW
Deepsleep1	On-chip peripheral registers are preserved. Cortex-A8 context/registers are lost, so the application needs to save them to the L3 OCMC RAM or DDR before entering DeepSleep. DDR is in self- refresh. For wake-up, boot ROM executes and branches to syste	Power supplies: • All power supplies are ON. • VDD_MPU = 0.95 V (nom) • VDD_CORE = 0.95 V (nom) Clocks: • Main Oscillator (OSC0) = OFF • All DPLLs are in bypass. Power domains: • PD_PER = ON • PD_MPU = OFF • PD_GFX = OFF • PD_WKUP = ON DDR is in self-refresh.	6.0	10.0	
Deepsleep0	PD_PER peripheral and Cortex-A8/MPU register information will be lost. On- chip peripheral register (context) information of PD-PER domain needs to be saved by application to SDRAM before entering this mode. DDR is in self- refresh. For wake-up, boot ROM executes and branches to peripheral context restore followed by system resume.	Power supplies: • All power supplies are ON. • VDD_MPU = 0.95 V (nom) • VDD_CORE = 0.95 V (nom) Clocks: • Main Oscillator (OSC0) = OFF • All DPLLs are in bypass. Power domains: • PD_PER = OFF • PD_MPU = OFF • PD_GFX = OFF • PD_WKUP = ON DDR is in self-refresh.	3.0	4.3	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JEP155	–	Recommended ESD Target Levels For HBM/MM Qualification
JEP157	–	Recommended ESD-CDM Target Levels
JESD 51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD 51-3	–	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-9	–	Test Boards for Area Array Surface Mount Package Thermal Measurements.
JESD79-2F	–	DDR2 SDRAM specification.
JESD79-3F	–	DDR2 SDRAM specification.
JESD209B	–	Low Power Double Data Rate (LPDDR).

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Functional block diagram. The functional block diagram shall be as shown in figure 2.

3.5.3 Pin Map Location (Section Left). Pin Map Location (Section Left) shall be as shown in figure 3.

3.5.4 Pin Map Location (Section Middle). Pin Map Location (Section Middle) shall be as shown in figure 4.

3.5.5 Pin Map Location (Section Right). Pin Map Location (Section Right) shall be as shown in figure 5.

3.5.6 Power Supply and Slew Rate. The Power Supply and Slew Rate shall be as shown in figure 6.

3.5.7 Preferred Power Supply Sequencing with Dual Voltage IOs Configured as 3.3 V. The Preferred Power Supply Sequencing with Dual Voltage IOs Configured as 3.3 V shall be as shown in figure 7.

3.5.8 Alternate Power Supply Sequencing with Dual Voltage IOs Configured as 3.3 V. The Alternate Power Supply Sequencing with Dual Voltage IOs Configured as 3.3 V shall be as shown in figure 8.

3.5.9 Power Supply Sequencing with Dual Voltage IOs Configured as 1.8 V. The Power Supply Sequencing with Dual Voltage IOs Configured as 1,8 V shall be as shown in figure 9.

3.5.10 Power-Supply Sequencing With Internal RTC LDO Disabled. The Power-Supply Sequencing With Internal RTC LDO Disabled shall be as shown in figure 10.

3.5.11 Power-Supply Sequencing with RTC Feature Disabled. The Power-Supply Sequencing with RTC Feature Disabled shall be as shown in figure 11.

3.5.12 VDD_MPU_MON Connectivity. The VDD_MPU_MON Connectivity shall be as shown in figure 12.

3.5.13 DPLL Power Supply Connectivity. The DPLL Power Supply Connectivity shall be as shown in figure 13.

3.5.14 OSC0 Start-Up Time. The OSC0 Start-Up Time shall be as shown in figure 14.

3.5.15 OSC1 Start-Up Time. The OSC1 Start-Up Time shall be as shown in figure 15.

3.5.16 OSC1 LVCMOS Circuit Schematic. The OSC1 LVCMOS Circuit Schematic shall be as shown in figure 16.

3.5.17 DCANx Timings. The DCANx Timings shall be as shown in figure 17.

3.5.18 Timer Timing. The Timer Timing shall be as shown in figure 18.

3.5.19 MDIO_DATA Timing - Input Mode. The MDIO_DATA Timing - Input Mode shall be as shown in figure 19.

3.5.20 MDIO_CLK Timing. The MDIO_CLK Timing shall be as shown in figure 20.

3.5.21 MDIO_DATA Timing - Output Mode. The MDIO_DATA Timing - Output Mode shall be as shown in figure 21.

3.5.22 GMII[x]_RXCLK Timing - MII Mode. The GMII[x]_RXCLK Timing - MII Mode shall be as shown in figure 22.

3.5.23 GMII[x]_TXCLK Timing - MII Mode. The GMII[x]_TXCLK Timing - MII Mode shall be as shown in figure 23.

3.5.24 GMII[x]_RXD[3:0], GMII[x]_RXDV, GMII[x]_RXER Timing - MII Mode. The GMII[x]_RXD[3:0], GMII[x]_RXDV, GMII[x]_RXER Timing - MII Mode shall be as shown in figure 24.

3.5.25 GMII[x]_TXD[3:0], GMII[x]_TXEN Timing - MII Mode. The GMII[x]_TXD[3:0], GMII[x]_TXEN Timing - MII Mode shall be as shown in figure 25.

3.5.26 RMII[x]_REFCLK Timing - RMII Mode. The RMII[x]_REFCLK Timing - RMII Mode shall be as shown in figure 26.

3.5.27 RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RXER Timing - RMII Mode. The RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RXER Timing - RMII Mode shall be as shown in figure 27.

3.5.28 RMII[x]_TXD[1:0], RMII[x]_TXEN Timing - RMII Mode. The RMII[x]_TXD[1:0], RMII[x]_TXEN Timing - RMII Mode shall be as shown in figure 28.

3.5.29 RGMII[x]_RCLK Timing - RGMII Mode. The RGMII[x]_RCLK Timing - RGMII Mode shall be as shown in figure 29.

3.5.30 RGMII[x]_RD[3:0], RGMII[x]_RCTL Timing - RGMII Mode. The RGMII[x]_RD[3:0], RGMII[x]_RCTL Timing - RGMII Mode shall be as shown in figure 30.

3.5.31 RGMII[x]_TCLK Timing - RGMII Mode. The RGMII[x]_TCLK Timing - RGMII Mode shall be as shown in figure 31.

3.5.32 RGMII[x]_TD[3:0], RGMII[x]_TCTL Timing - RGMII Mode. The RGMII[x]_TD[3:0], RGMII[x]_TCTL Timing - RGMII Mode shall be as shown in figure 32.

3.5.33 GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0). The GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0) shall be as shown in figure 33.

3.5.34 GPMC and NOR Flash—Synchronous Burst Read—4x16-bit (GpmcFCLKDivider = 0). The GPMC and NOR Flash—Synchronous Burst Read—4x16-bit (GpmcFCLKDivider = 0) shall be as shown in figure 34.

3.5.35 GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0). The GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0) shall be as shown in figure 35.

3.5.36 GPMC and Multiplexed NOR Flash—Synchronous Burst Read. The GPMC and Multiplexed NOR Flash—Synchronous Burst Read shall be as shown in figure 36.

3.5.37 GPMC and Multiplexed NOR Flash—Synchronous Burst Write. The GPMC and Multiplexed NOR Flash—Synchronous Burst Write shall be as shown in figure 37.

3.5.38 GPMC and NOR Flash—Asynchronous Read—Single Word. The GPMC and NOR Flash—Asynchronous Read—Single Word shall be as shown in figure 38.

3.5.39 GPMC and NOR Flash—Asynchronous Read—32-bit. The GPMC and NOR Flash—Asynchronous Read—32-bit shall be as shown in figure 39.

3.5.40 GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-bit. The GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-bit shall be as shown in figure 40.

3.5.41 GPMC and NOR Flash—Asynchronous Write—Single Word. The GPMC and NOR Flash—Asynchronous Write—Single Word shall be as shown in figure 41.

3.5.42 GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word. The GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word shall be as shown in figure 42.

3.5.43 GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word. The GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word shall be as shown in figure 43.

3.5.44 GPMC and NAND Flash—Command Latch Cycle. The GPMC and NAND Flash—Command Latch Cycle shall be as shown in figure 44.

3.5.45 GPMC and NAND Flash—Address Latch Cycle. The GPMC and NAND Flash—Address Latch Cycle shall be as shown in figure 45.

3.5.46 GPMC and NAND Flash—Data Read Cycle. The GPMC and NAND Flash—Data Read Cycle shall be as shown in figure 46.

3.5.47 GPMC and NAND Flash— Data Write Cycle. The GPMC and NAND Flash— Data Write Cycle shall be as shown in figure 47.

3.5.48 LPDDR Memory Interface Clock Timing. The LPDDR Memory Interface Clock Timing shall be as shown in figure 48.

3.5.49 AM3358-EP Device and LPDDR Device Placement. The AM3358-EP Device and LPDDR Device Placement shall be as shown in figure 49.

3.5.50 CK and ADDR_CTRL Routing and Topology. The CK and ADDR_CTRL Routing and Topology shall be as shown in figure 50.

3.5.51 DQS[x] and DQ[x] Routing and Topology. The DQS[x] and DQ[x] Routing and Topology shall be as shown in figure 51.

3.5.52 DDR2 Memory Interface Clock Timing. The DDR2 Memory Interface Clock Timing shall be as shown in figure 52.

3.5.53 AM3358-EP Device and DDR2 Device Placement. The AM3358-EP Device and DDR2 Device Placement shall be as shown in figure 53.

3.5.54 CK and ADDR_CTRL Routing and Topology. The CK and ADDR_CTRL Routing and Topology shall be as shown in figure 54.

3.5.55 DQS[x] and DQ[x] Routing and Topology. The DQS[x] and DQ[x] Routing and Topology shall be as shown in figure 55.

3.5.56 DDR3 Memory Interface Clock Timing. The DDR3 Memory Interface Clock Timing shall be as shown in figure 56.

3.5.57 Placement Specifications. The Placement Specifications shall be as shown in figure 57.

3.5.58 CLM for Two Address Loads on One Side of PCB. The CLM for Two Address Loads on One Side of PCB shall be as shown in figure 58.

3.5.59 DQLM for Any Number of Allowed DDR3 Devices. The DQLM for Any Number of Allowed DDR3 Devices shall be as shown in figure 59.

3.5.60 I^2C Receive Timing. The I^2C Receive Timing shall be as shown in figure 60.

3.5.61 I^2C Transmit Timing. The I^2C Transmit Timing shall be as shown in figure 61.

3.5.62 JTAG Timing. The JTAG Timing shall be as shown in figure 62.

3.5.63 Command Write in Hitachi Mode. The Command Write in Hitachi Mode shall be as shown in figure 63.

3.5.64 Data Write in Hitachi Mode. The Data Write in Hitachi Mode shall be as shown in figure 64.

3.5.65 Command Read in Hitachi Mode. The Command Read in Hitachi Mode shall be as shown in figure 65.

3.5.66 Data Read in Hitachi Mode. The Data Read in Hitachi Mode shall be as shown in figure 66.

3.5.67 Micro-Interface Graphic Display Motorola Write. The Micro-Interface Graphic Display Motorola Write shall be as shown in figure 67.

3.5.68 Micro-Interface Graphic Display Motorola Read. The Micro-Interface Graphic Display Motorola Read shall be as shown in figure 68.

3.5.69 Micro-Interface Graphic Display Motorola Status. The Micro-Interface Graphic Display Motorola Status shall be as shown in figure 69.

3.5.70 Micro-Interface Graphic Display Intel Write. The Micro-Interface Graphic Display Intel Write shall be as shown in figure 70.

3.5.71 Micro-Interface Graphic Display Intel Read. The Micro-Interface Graphic Display Intel Read shall be as shown in figure 71.

3.5.72 Micro-Interface Graphic Display Intel Status. The Micro-Interface Graphic Display Intel Status shall be as shown in figure 72.

3.5.73 LCD Raster-Mode Active. The LCD Raster-Mode Active shall be as shown in figure 73.

3.5.74 LCD Raster-Mode Passive. The LCD Raster-Mode Passive shall be as shown in figure 74.

3.5.75 LCD Raster-Mode Control Signal Activation. The LCD Raster-Mode Control Signal Activation shall be as shown in figure 75.

3.5.76 LCD Raster-Mode Control Signal Deactivation. The LCD Raster-Mode Control Signal Deactivation shall be as shown in figure 76.

3.5.77 McASP Input Timing. The McASP Input Timing shall be as shown in figure 77.

3.5.78 McASP Input Timing. The McASP Input Timing shall be as shown in figure 78.

3.5.79 McASP Output Timing. The McASP Output Timing shall be as shown in figure 79.

3.5.80 SPI Slave Mode Receive Timing. The SPI Slave Mode Receive Timing shall be as shown in figure 80.

3.5.81 SPI Slave Mode Transmit Timing. The SPI Slave Mode Transmit Timing shall be as shown in figure 81.

3.5.82 SPI Master Mode Receive Timing. The SPI Master Mode Receive Timing shall be as shown in figure 82.

3.5.83 SPI Master Mode Transmit Timing. The SPI Master Mode Transmit Timing shall be as shown in figure 83.

3.5.84 MMC[x]_CMD and MMC[x]_DAT[7:0] Input Timing. The MMC[x]_CMD and MMC[x]_DAT[7:0] Input Timing shall be as shown in figure 84.

3.5.85 MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—Standard Mode. The MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—Standard Mode shall be as shown in figure 85.

3.5.86 MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—High Speed Mode. The MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—High Speed Mode shall be as shown in figure 86.

3.5.87 PRU-ICSS PRU Direct Input Timing. The PRU-ICSS PRU Direct Input Timing shall be as shown in figure 87.

3.5.88 PRU-ICSS PRU Direct Output Timing. The PRU-ICSS PRU Direct Output Timing shall be as shown in figure 88.

3.5.89 PRU-ICSS PRU Parallel Capture Timing - Rising Edge Mode. The PRU-ICSS PRU Parallel Capture Timing - Rising Edge Mode shall be as shown in figure 89.

3.5.90 PRU-ICSS PRU Parallel Capture Timing - Falling Edge Mode. The PRU-ICSS PRU Parallel Capture Timing - Falling Edge Mode shall be as shown in figure 90.

3.5.91 PRU-ICSS PRU Shift In Timing. The PRU-ICSS PRU Shift In Timing shall be as shown in figure 91.

3.5.92 PRU-ICSS PRU Shift Out Timing. The PRU-ICSS PRU Shift Out Timing shall be as shown in figure 92.

3.5.93 PRU-ICSS MDIO_DATA Timing - Input Mode. The PRU-ICSS MDIO_DATA Timing - Input Mode shall be as shown in figure 93.

3.5.94 PRU-ICSS MDIO_CLK Timing. The PRU-ICSS MDIO_CLK Timing shall be as shown in figure 94.

3.5.95 PRU-ICSS MDIO_DATA Timing – Output Mode. The PRU-ICSS MDIO_DATA Timing – Output Mode shall be as shown in figure 95.

3.5.96 PRU-ICSS MII_RXCLK Timing. The PRU-ICSS MII_RXCLK Timing shall be as shown in figure 96.

3.5.97 PRU-ICSS MII_TXCLK Timing**.** The PRU-ICSS MII_TXCLK Timing shall be as shown in figure 97.

3.5.98 PRU-ICSS MII_RXD[3:0], MII_RXDV, and MII_RXER Timing**.** The PRU-ICSS MII_RXD[3:0], MII_RXDV, and MII_RXER Timing shall be as shown in figure 98.

3.5.99 PRU-ICSS MII_TXD[3:0], MII_TXEN Timing**.** The PRU-ICSS MII_TXD[3:0], MII_TXEN Timing shall be as shown in figure 99.

3.5.100 PRU-ICSS UART Timing**.** The PRU-ICSS UART Timing shall be as shown in figure 100.

3.5.101 UART Timing**.** The UART Timing shall be as shown in figure 101.

3.5.102 UART IrDA Pulse Parameters**.** The UART IrDA Pulse Parameters shall be as shown in figure 102.

TABLE I. Electrical performance characteristics. 1/ 2/ 3/

Test		Symbol	Limits			Unit
			Min	Typ	Max	
DC Electrical Characteristics 3/						
DDR_RESETn,DDR_CSn0,DDR_CKE,DDR_CK,DDR_CKn,DDR_CASn,DDR_RASn,DDR_WEn,DDR_BA0,DDR_BA1,DDR_BA2, DDR_A0,DDR_A1,DDR_A2,DDR_A3,DDR_A4,DDR_A5,DDR_A6,DDR_A7,DDR_A8,DDR_A9,DDR_A10,DDR_A11,DDR_A12, DDR_A13,DDR_A14,DDR_A15,DDR_ODT,DDR_D0,DDR_D1,DDR_D2,DDR_D3,DDR_D4,DDR_D5,DDR_D6,DDR_D7,DDR_D8, DDR_D9,DDR_D10, DDR_D11,DDR_D12,DDR_D13,DDR_D14,DDR_D15,DDR_DQM 0,DDR_DQM1,DDR_DQS0, DDR_DQSn0,DDR_DQS1,DDR_DQSn1 Pins						
High-level input voltage		V_{IH}	0.65 × VDDS_DDR			V
Low-level input voltage		V_{IL}			0.35 × VDDS_DDR	V
Hysteresis voltage at an input		V_{HYS}	0.07		0.25	V
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 8 mA	V_{OH}	VDDS_DDR – 0.4			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 8 mA	V_{OL}			0.4	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			10	µA
Input leakage current, Receiver disabled, pullup enabled			-240		-80	
Input leakage current, Receiver disabled, pulldown enabled			80		240	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}			10	µA
DDR_RESETn,DDR_CSn0,DDR_CKE,DDR_CK,DDR_CKn,DDR_CASn,DDR_RASn,DDR_WEn,DDR_BA0,DDR_BA1,DDR_BA2, DDR_A0,DDR_A1,DDR_A2,DDR_A3,DDR_A4,DDR_A5,DDR_A6,DDR_A7,DDR_A8,DDR_A9,DDR_A10,DDR_A11,DDR_A12, DDR_A13,DDR_A14,DDR_A15, DDR_ODT,DDR_D0,DDR_D1,DDR_D2,DDR_D3,DDR_D4,DDR_D5,DDR_D6,DDR_D7,DDR_D8, DDR_D9,DDR_D10,DDR_D11,DDR_D12,DDR_D13,DDR_D14, DDR_D15,DDR_DQM0,DDR_DQM1,DDR_DQS0, DDR_DQSn0, DDR_DQS1,DDR_DQSn1 Pins (DDR2 - SSTL Mode)						
High-level input voltage		V_{IH}	DDR_VREF + 0.125			V
Low-level input voltage		V_{IL}			DDR_VREF – 0.125	V
Hysteresis voltage at an input		V_{HYS}		N/A		V
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 8 mA	V_{OH}	VDDS_DDR – 0.4			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 8 mA	V_{OL}			0.4	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			10	µA
Input leakage current, Receiver disabled, pullup enabled			-240		-80	
Input leakage current, Receiver disabled, pulldown enabled			80		240	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}			10	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

Test		Symbol	Limits			Unit
			Min	Typ	Max	
DC Electrical Characteristics (Continued) 3/						
DDR_RESETn,DDR_CSn0,DDR_CKE,DDR_CK,DDR_CKn,DDR_CASn,DDR_RASn,DDR_WEn,DDR_BA0,DDR_BA1,DDR_BA2, DDR_A0,DDR_A1,DDR_A2,DDR_A3,DDR_A4,DDR_A5,DDR_A6,DDR_A7,DDR_A8,DDR_A9,DDR_A10,DDR_A11,DDR_A12, DDR_A13,DDR_A14,DDR_A15,DDR_ODT,DDR_D0,DDR_D1,DDR_D2,DDR_D3,DDR_D4,DDR_D5,DDR_D6,DDR_D7, DDR_D8,DDR_D9,DDR_D10,DDR_D11,DDR_D12,DDR_D13,DDR_D14,DDR_D15,DDR_DQM0,DDR_DQM1,DDR_DQS0, DDR_DQSn0,DDR_DQS1,DDR_DQSn1 Pins (DDR3, DDR3L - HSTL Mode)						
High-level input voltage	VDDS_DDR = 1.5 V	V_{IH}	DDR_VREF + 0.1			V
	VDDS_DDR = 1.35 V		DDR_VREF + 0.09			
Low-level input voltage	VDDS_DDR = 1.5 V	V_{IL}			DDR_VREF – 0.1	V
	VDDS_DDR = 1.35 V				DDR_VREF – 0.09	
Hysteresis voltage at an input		V_{HYS}		N/A		V
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 8 mA	V_{OH}	VDDS_DDR – 0.4			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 8 mA	V_{OL}			0.4	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			10	µA
Input leakage current, Receiver disabled, pullup enabled			-240		-80	
Input leakage current, Receiver disabled, pulldown enabled			80		240	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}			10	µA
ECAP0_IN_PWM0_OUT,UART0_CTSn,UART0_RTSn,UART0_RXD,UART0_TXD,UART1_CTSn,UART1_RTSn,UART1_RXD, UART1_TXD,I2C0_SDA,I2C0_SCL,XDMA_EVENT_INTR0,XDMA_EVENT_INTR1,WARMRSTn,EXTINTn,TMS,TDO, USB0_DRVVBUS,USB1_DRVVBUS (VDDSHV6 = 1.8 V)						
High-level input voltage		V_{IH}	0.65 × VDDSHV6			V
Low-level input voltage		V_{IL}			0.35 × VDDSHV6	V
Hysteresis voltage at an input		V_{HYS}	0.18		0.305	V
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 4 mA	V_{OH}	VDDSHV6 – 0.45			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 4 mA	V_{OL}			0.45	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			8	µA
Input leakage current, Receiver disabled, pullup enabled			-161	-100	-52	
Input leakage current, Receiver disabled, pulldown enabled			52	100	170	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}			8	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

Test		Symbol	Limits			Unit
			Min	Typ	Max	
DC Electrical Characteristics (Continued) 3/						
ECAP0_IN_PWM0_OUT,UART0_CTSn,UART0_RTSn,UART0_RXD,UART0_TXD,UART1_CTSn,UART1_RTSn,UART1_RXD, UART1_TXD,I2C0_SDA,I2C0_SCL,XDMA_EVENT_INTR0,XDMA_EVENT_INTR1,WARMRSTn,EXTINTn,TMS,TDO, USB0_DRVVBUS,USB1_DRVVBUS (VDDSHV6 = 3.3 V)						
High-level input voltage		V_{IH}	2			V
Low-level input voltage		V_{IL}			0.8	V
Hysteresis voltage at an input		V_{HYS}	0.265		0.44	V
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 8 mA	V_{OH}	VDDSHV6 – 0.45			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 8 mA	V_{OL}			0.45	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			18	µA
Input leakage current, Receiver disabled, pullup enabled			-243	-100	-19	
Input leakage current, Receiver disabled, pulldown enabled			51	110	210	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}			18	µA
TCK (VDDSHV6 = 1.8 V)						
High-level input voltage		V_{IH}	1.45			V
Low-level input voltage		V_{IL}			0.46	V
Hysteresis voltage at an input		V_{HYS}	0.4			V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			8	µA
Input leakage current, Receiver disabled, pullup enabled			-161	-100	-52	
Input leakage current, Receiver disabled, pulldown enabled			52	100	170	
TCK (VDDSHV6 = 3.3 V)						
High-level input voltage		V_{IH}	2.15			V
Low-level input voltage		V_{IL}			0.46	V
Hysteresis voltage at an input		V_{HYS}	0.4			V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			18	µA
Input leakage current, Receiver disabled, pullup enabled			-243	-100	-19	
Input leakage current, Receiver disabled, pulldown enabled			51	110	210	
PWRONRSTn (VDDSHV6 = 1.8 or 3.3 V) 4/						
High-level input voltage		V_{IH}	1.35			V
Low-level input voltage		V_{IL}			0.5	V
Hysteresis voltage at an input		V_{HYS}	0.07			V
Input leakage current	V_I = 1.8 V	I_I			0.1	µA
	V_I = 3.3 V				2	

See footnote at end of table.

TABLE I. Electrical performance characteristics- Continued. 1/ 2/ 3/

Test		Symbol	Limits			Unit
			Min	Typ	Max	
DC Electrical Characteristics (Continued) 3/						
RTC_PWRONRSTn						
High-level input voltage		V_{IH}	0.65 × VDDS_RTC			V
Low-level input voltage		V_{IL}			0.35 × VDDS_RTC	V
Hysteresis voltage at an input		V_{HYS}	0.065			V
Input leakage current		I_I	-1		1	µA
PMIC_POWER_EN						
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 6 mA	V_{OH}	VDDS_RTC – 0.45			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 6 mA	V_{OL}			0.45	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I	-1		1	µA
Input leakage current, Receiver disabled, pullup enabled			-200		-40	
Input leakage current, Receiver disabled, pulldown enabled			40		200	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}	-1		1	µA
EXT_WAKEUP						
High-level input voltage		V_{IH}	0.65 × VDDS_RTC			V
Low-level input voltage		V_{IL}			0.35 × VDDS_RTC	V
Hysteresis voltage at an input		V_{HYS}	0.15			V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I	-1		1	µA
Input leakage current, Receiver disabled, pullup enabled			-200		-40	
Input leakage current, Receiver disabled, pulldown enabled			40		200	
XTALIN (OSC0)						
High-level input voltage		V_{IH}	0.65 × VDDS_OSC			V
Low-level input voltage		V_{IL}			0.35 × VDDS_OSC	V
RTC_XTALIN (OSC1)						
High-level input voltage		V_{IH}	0.65 × VDDS_RTC			V
Low-level input voltage		V_{IL}			0.35 × VDDS_RTC	V

See footnote at end of table.

TABLE I. Electrical performance characteristics- Continued. 1/ 2/ 3/

Test		Symbol	Limits			Unit
			Min	Typ	Max	
DC Electrical Characteristics (Continued) 3/						
All other LVCMOS pins (VDDSHVx = 1.8 V; x = 1 to 6)						
High-level input voltage		V_{IH}	0.65 × VDDSHVx			V
Low-level input voltage		V_{IL}			0.35 × VDDSHVx	V
Hysteresis voltage at an input		V_{HYS}	0.18		0.305	V
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 6 mA	V_{OH}	VDDSHVx – 0.45			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 6 mA	V_{OL}			0.45	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			8	µA
Input leakage current, Receiver disabled, pullup enabled			-161	-100	-52	
Input leakage current, Receiver disabled, pulldown enabled			52	100	170	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}			8	µA
All other LVCMOS pins (VDDSHVx = 3.3 V; x = 1 to 6)						
High-level input voltage		V_{IH}	2			V
Low-level input voltage		V_{IL}			0.8	V
Hysteresis voltage at an input		V_{HYS}	0.265		0.44	V
High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 6 mA	V_{OH}	VDDSHVx – 0.45			V
Low level output voltage, driver enabled, pullup orpulldown disabled	I_{OL} = 6 mA	V_{OL}			0.45	V
Input leakage current, Receiver disabled, pullup or pulldown inhibited		I_I			18	µA
Input leakage current, Receiver disabled, pullup enabled			-243	-100	-19	
Input leakage current, Receiver disabled, pulldown enabled			51	110	210	
Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		I_{OZ}			18	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
5.9 External Capacitors						
Core Voltage Decoupling Characteristics						
C_{VDD_COR} 5/				10.08		µF
C_{VDD_MPU} 6/				10.05		
Power-Supply Decoupling Capacitor Characteristics						
C_{VDDA_ADC}				10		nF
$C_{VDDA1P8V\_USB0}$				10		
$C_{CVDDA3P3V\_USB0}$				10		
$C_{VDDA3P3V\_USB1}$				10		
C_{VDDS} 7/				10.04		µF
C_{VDDS_DDR}				8/		
C_{VDDS_OSC}				10		nF
$C_{VDDS\_PLL\_DDR}$				10		
$C_{VDDS\_PLL\_CORE\_LCD}$				10		
$C_{VDDS\_SRAM\_CORE\_BG}$ 9/				10.01		µF
$C_{VDDS\_SRAM\_MPU\_BB}$ 10/				10.01		
$C_{VDDS\_PLL\_MPU}$				10		
C_{VDDS_RTC}				10		
$C_{VDDSHV1}$ 11/				10.02		
$C_{VDDSHV2}$ 11/				10.02		
$C_{VDDSHV3}$ 11/				10.02		
$C_{VDDSHV4}$ 11/				10.02		
$C_{VDDSHV5}$ 11/				10.02		
$C_{VDDSHV6}$ 12/				10.06		
Output Capacitor Characteristics						
$C_{CAP\_VDD\_SRAM\_CORE}$ 13/				1		µF
$C_{CAP\_VDD\_RTC}$ 13/ 14/				1		
$C_{CAP\_VDD\_SRAM\_MPU}$ 13/				1		
$C_{CAP\_VBB\_MPU}$ 13/				1		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
Touch Screen Controller and Analog-to-Digital Subsystem Electrical Parameters					
TSC_ADC Electrical Parameters					
Analog Input					
VREFP 15/		(0.5 × VDDA_ADC) + 0.25		VDDA_ADC	V
VREFN 15/		0		(0.5 × VDDA_ADC) – 0.25	V
VREFP + VREFN 15/			VDDA_ADC		V
Full-scale input range	Internal voltage reference	0		VDDA_ADC	V
	External voltage reference	VREFN		VREFP	V
Differential non-linearity (DNL)	Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V	-1	0.5	1	LSB
Integral non-linearity (INL)	Source impedance = 50 Ω Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V	-2	±1	2	LSB
	Source impedance = 1 kΩ Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V		±1		LSB
Gain error	Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V		±2		LSB
Offset error	Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V		±2		LSB
Input sampling capacitance			5.5		pF
Signal-to-noise ratio (SNR)	Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale		70		dB
Total harmonic distortion THD)	Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale		75		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
Touch Screen Controller and Analog-to-Digital Subsystem Electrical Parameters - Continued					
TSC_ADC Electrical Parameters - Continued					
Spurious free dynamic range	Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale		80		dB
Signal-to-noise plus distortion	Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale		69		dB
VREFP and VREFN input impedance			20		kΩ
Input impedance of AIN[7:0] 15/			[1 / ((65.97 × 10–12) × f)]		Ω
Sampling Dynamics					
Conversion time		15			ADC Clock cycles
Acquisition time		2			
Sampling rate	ADC clock = 3 MHz		200		kSPS
Channel-to-channel isolation			100		dB
Touch Screen Switch Drivers					
Pull-up and pull-down switch ON resistance (Ron)			2		Ω
Pull-up and pull-down switch current leakage Ileak	Source impedance = 500 Ω			0.5	uA
Drive current				25	mA
Touch screen resistance				6	kΩ
Pen touch detect				2	kΩ

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

SUPPLY NAME	DESCRIPTION	Limits			Unit
		Min	Typ	Max	
Power and Clocking (See Figure 6 to Figure 12)					
Digital Phase-Locked Loop Power Supply Requirements					
DPLL Power Supply Requirements (See Figure 13)					
VDDA1P8V_USB0	Supply voltage range for USBPHY and PER DPLL, Analog, 1.8 V	1.71	1.8	1.89	V
	Max peak-to-peak supply noise			50	mV (p-p)
VDDS_PLL_MPU	Supply voltage range for DPLL MPU, analog	1.71	1.8	1.89	V
	Max peak-to-peak supply noise			50	mV (p-p)
VDDS_PLL_CORE_LCD	Supply voltage range for DPLL CORE and LCD, analog	1.71	1.8	1.89	V
	Max peak-to-peak supply noise			50	mV (p-p)
VDDS_PLL_DDR	Supply voltage range for DPLL DDR, analog	1.71	1.8	1.89	V
	Max peak-to-peak supply noise			50	mV (p-p)

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Power and Clocking – Continued. Clock Specifications						
OSC0 Crystal Circuit Requirements						
Crystal parallel resonance frequency	$f$xtal	Fundamental mode oscillation only		19.2, 24, 25 or 26		MHz
Crystal frequency stability and tolerance 17/			-50		50	ppm
C1 capacitance	C_{C1}	C_{shunt} ≤ 5 pF	12		24	pF
		C_{shunt} > 5 pF	18		24	
C2 capacitance	C_{C2}	C_{shunt} ≤ 5 pF	12		24	
		C_{shunt} > 5 pF	18		24	
Shunt capacitance	Cshunt				7	pF
Crystal effective series resistance	ESR	$f$xtal = 19.2 MHz, oscillator has nominal negative resistance of 272 Ω and worstcase negative resistance of 163 Ω			54.5	Ω
		$f$xtal = 24 MHz, oscillator has nominal negative resistance of 240 Ω and worstcase negative resistance of 144 Ω			48.0	
		$f$xtal = 25 MHz, oscillator has nominal negative resistance of 233 Ω and worstcase negative resistance of 140 Ω			46.6	
		$f$xtal = 26 MHz, oscillator has nominal negative resistance of 227 Ω and worstcase negative resistance of 137 Ω			45.3	
OSC0 Crystal Circuit Characteristics (See Figure 14)						
Shunt capacitance of package	C_{pkg}			0.01		pF
The actual values of the ESR, $f$xtal, and CL should be used to yield a typical crystal power dissipation value. Using the maximum values specified for ESR, $f$xtal, and CL parameters yields a maximum powerdissipation value.				18		
Start-up time	t_{sX}			1.5		ms
OSC0 LVCMOS Reference Clock Requirements						
Frequency, LVCMOS reference clock	$f_{(XTALIN)}$			19.2, 24, 25 or 26		MHz
Frequency, LVCMOS reference clock stability and tolerance 17/			-50		50	ppm
Duty cycle, LVCMOS reference clock period	$t_{dc(XTALIN)}$		45%		55%	
Jitter peak-to-peak, LVCMOS reference clock period	$t_{jpp(XTALIN)}$		-1%		1%	
Time, LVCMOS reference clock rise	$t_{R(XTALIN)}$				5	ns
Time, LVCMOS reference clock fall	$t_{F(XTALIN)}$				5	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

DESCRIPTION		Symbol	Limits			Unit
			Min	Typ	Max	
Power and Clocking – Continued. **Clock Specifications**						
OSC1 Crystal Circuit Requirements						
Crystal parallel resonance frequency	Fundamental mode oscillation only	f_{xtal}		32.768		kHz
Crystal frequency stability and tolerance 17/	Maximum RTC error = 10.512 minutes per year		-20.0		20.0	ppm
	Maximum RTC error = 26.28 minutes per year		-50.0		50.0	ppm
C1 capacitance		C_{C1}	12.0		24.0	pF
C2 capacitance		C_{C2}	12.0		24.0	pF
Shunt capacitance		Cshunt			1.5	pF
Crystal effective series resistance	$f$xtal = 32.768 kHz, oscillator has nominal negative resistance of 725 kΩ and worstcase negative resistance of 250 kΩ	ESR			80	kΩ
OSC1 Crystal Circuit Characteristics (See Figure 15)						
Shunt capacitance of GCZ package		Cpkg		0.01		pF
The actual values of the ESR, $f$xtal, and CL should be used to yield a typical crystal power dissipation value. Using the maximum values specified for ESR, $f$xtal, and CL parameters yields a maximum power dissipation value.		P_{xtal}		20/		
Start-up time		t_{sX}		2		s
OSC1 LVCMOS Reference Clock Requirements (See Figure 16)						
Frequency, LVCMOS reference clock		$f_{(RTC\_XTALIN)}$		32.768		kHz
Frequency, LVCMOS reference clock 21/	Maximum RTC error =10.512 minutes/year		-20.0		20.0	ppm
	Maximum RTC error =26.28 minutes/year		-50.0		50.0	ppm
Duty cycle, LVCMOS reference clock period		$t_{dc(RTC\_XTALIN)}$	45%		55%	
Jitter peak-to-peak, LVCMOS reference clock period		$t_{jpp(RTC\_XTALIN)}$	-1%		1%	
Time, LVCMOS reference clock rise		$t_{R(RTC\_XTALIN)}$			5	ns
Time, LVCMOS reference clock fall		$t_{F(RTC\_XTALIN)}$			5	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

No	Test	Symbol	Limits			Unit
			Min	Typ	Max	
Peripheral Information and Timings						
Controller Area Network (CAN)						
Timing Requirements for DCANx Receive (See Figure 17)						
	Maximum programmable baud rate	$f_{baud(baud)}$			1	Mbps
1	Pulse duration, receive data bit	$t_{w(RX)}$	H – 2 22/		H + 2 22/	ns
Switching Characteristics for DCANx Transmit (See Figure 17)						
	Maximum programmable baud rate	$f_{baud(baud)}$			1	Mbps
2	Pulse duration, transmit data bit	$t_{w(TX)}$	H – 2 22/		H + 2 22/	ns
DMTimer Electrical Data and Timing						
Timing Requirements for DMTimer [1-7] (See Figure 18)						
1	Cycle time, TCLKIN	$t_{c(TCLKIN)}$	4P + 1 23/			ns
Switching Characteristics for DMTimer [4-7] (See Figure 18)						
2	Pulse duration, high	$tw_{(TIMERxH)}$	4P - 3 23/			ns
3	Pulse duration, low	$t_{w(TIMERxL)}$	4P - 3 23/			ns
Ethernet Media Access Controller (EMAC) and Switch						
EMAC and Switch Timing Conditions						
Input Conditions						
	Input signal rise time	t_R	1 24/		5 24/	ns
	Input signal fall time	t_F	1 24/		5 24/	ns
Output Condition						
	Output load capacitance	C_{LOAD}	3		30	pF
Timing Requirements for MDIO_DATA (See Figure 19)						
1	Setup time, MDIO valid before MDC high	$t_{su(MDIO-MDC)}$	90			ns
2	Hold time, MDIO valid from MDC high	$t_{h(MDIO-MDC)}$	0			ns
Switching Characteristics for MDIO_CLK (See Figure 20)						
1	Cycle time, MDC	$t_{c(MDC)}$	400			ns
2	Pulse duration, MDC high	$t_{w(MDCH)}$	160			ns
3	Pulse duration, MDC low	$t_{w(MDCL)}$	160			ns
4	Transition time, MDC	$t_{t(MDC)}$			5	ns
Switching Characteristics for MDIO_DATA (See Figure 21)						
1	Delay time, MDC high to MDIO valid	$t_{d(MDC-MDIO)}$	10		390	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

No	Test	Symbol	Limits						Unit
			10 Mbps			100 Mbps			
			Min	Typ	Max	Min	Typ	Max	
Peripheral Information and Timings - Continued									
Ethernet Media Access Controller (EMAC) and Switch – Continued.									
Timing Requirements for GMII[x]_RXCLK - MII Mode (See Figure 22)									
1	Cycle time, RX_CLK	$t_{c(RX\_CLK)}$	399.96		400.04	39.996		40.004	ns
2	Pulse duration, RX_CLK high	$t_{w(RX\_CLKH)}$	140		260	14		26	ns
3	Pulse duration, RX_CLK low	$t_{w(RX\_CLKL)}$	140		260	14		26	ns
4	Transition time, RX_CLK	$t_{t(RX\_CLK)}$			5			5	ns
Timing Requirements for GMII[x]_TXCLK - MII Mode (See Figure 23)									
1	Cycle time, TX_CLK	$t_{c(TX\_CLK)}$	399.96		400.04	39.996		40.004	ns
2	Pulse duration, TX_CLK high	$t_{w(TX\_CLKH)}$	140		260	14		26	ns
3	Pulse duration, TX_CLK low	$t_{w(TX\_CLKL)}$	140		260	14		26	ns
4	Transition time, TX_CLK	$t_{t(TX\_CLK)}$			5			5	ns
Timing Requirements for GMII[x]_RXD[3:0], GMII[x]_RXDV, and GMII[x]_RXER - MII Mode (See Figure 24)									
1	Setup time, RXD[3:0] valid before RX_CLK	$t_{su(RXD-RX\_CLK)}$	8			8			ns
	Setup time, RX_DV valid before RX_CLK	$t_{su(RX\_DV-RX\_CLK)}$							
	Setup time, RX_ER valid before RX_CLK	$t_{su(RX\_ER-RX\_CLK)}$							
2	Hold time RXD[3:0] valid after RX_CLK	$t_{h(RX\_CLK-RXD)}$	8			8			ns
	Hold time RX_DV valid after RX_CLK	$t_{h(RX\_CLK-RX\_DV)}$							
	Hold time RX_ER valid after RX_CLK	$t_{h(RX\_CLK-RX\_ER)}$							
Switching Characteristics for GMII[x]_TXD[3:0], and GMII[x]_TXEN - MII Mode (See Figure 25)									
1	Delay time, TX_CLK high to TXD[3:0] valid	$td_{(TX\_CLK-TXD)}$	5		25	5		25	ns
	Delay time, TX_CLK to TX_EN valid	$t_{d(TX\_CLK-TX\_EN)}$							

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

No	Test	Symbol	Limits			Unit
			Min	Typ	Max	
Peripheral Information and Timings - Continued						
Ethernet Media Access Controller (EMAC) and Switch – Continued.						
Timing Requirements for RMII[x]_REFCLK - RMII Mode (See Figure 26)						
1	Cycle time, REF_CLK	$t_{c(REF\_CLK)}$	19.999		20.001	ns
2	Pulse duration, REF_CLK high	$t_{w(REF\_CLKH)}$	7		13	ns
3	Pulse duration, REF_CLK low	$t_{w(REF\_CLKL)}$	7		13	ns
Timing Requirements for RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER - RMII Mode (See Figure 27)						
1	Setup time, RXD[1:0] valid before REF_CLK	$t_{su(RXD-REF\_CLK)}$	4			ns
	Setup time, CRS_DV valid before REF_CLK	$t_{su(CRS\_DV-REF\_CLK)}$				
	Setup time, RX_ER valid before REF_CLK	$t_{su(RX\_ER-REF\_CLK)}$				
2	Hold time RXD[1:0] valid after REF_CLK	$t_{h(REF\_CLK-RXD)}$	2			ns
	Hold time, CRS_DV valid after REF_CLK	$t_{h(REF\_CLK-CRS\_DV)}$				
	Hold time, RX_ER valid after REF_CLK	$t_{h(REF\_CLK-RX\_ER)}$				
Switching Characteristics for RMII[x]_TXD[1:0], and RMII[x]_TXEN - RMII Mode (See Figure 28)						
1	Delay time, REF_CLK high to TXD[1:0] valid	$t_{d(REF\_CLK-TXD)}$	2		13	ns
	Delay time, REF_CLK to TXEN valid	$td_{(REF\_CLK-TXEN)}$				
2	Rise time, TXD outputs	$t_{r(TXD)}$	1		5	ns
	Rise time, TX_EN output	$t_{r(TX\_EN)}$				
3	Fall time, TXD outputs	$t_{f(TXD)}$	1		5	ns
	Fall time, TX_EN output	$t_{f(TX\_EN)}$				

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/

No	Test	Symbol	Limits						Unit
			10 Mps		100 Mps		1000 Mps		
			Min	Max	Min	Max	Min	Max	
Peripheral Information and Timings - Continued									
Ethernet Media Access Controller (EMAC) and Switch – Continued.									
Timing Requirements for RGMII[x]_RCLK - RGMII Mode (See Figure 29)									
1	Cycle time, RXC	$t_{c(RXC)}$	360	440	36	44	7.2	8.8	ns
2	Pulse duration, RXC high	$t_{w(RXCH)}$	160	240	16	24	3.6	4.4	ns
3	Pulse duration, RXC low	$t_{w(RXCL)}$	160	240	16	24	3.6	4.4	ns
4	Transition time, RXC	$t_{t(RXC)}$		0.75		0.75		0.75	ns
Timing Requirements for RGMII[x]_RD[3:0], and RGMII[x]_RCTL - RGMII Mode (See Figure 30)									
1	Setup time, RD[3:0] valid before RXC high or low	$t_{su(RD-RXC)}$	1		1		1		ns
	Setup time, RX_CTL valid before RXC high or low	$t_{su(RX\_CTL-RXC)}$	1		1		1		ns
2	Hold time, RD[3:0] valid after RXC high or low	$t_{h(RXC-RD)}$	1		1		1		ns
	Hold time, RX_CTL valid after RXC high or low	$t_{h(RXC-RX\_CTL)}$	1		1		1		ns
3	Transition time, RD	$t_{t(RD)}$		0.75		0.75		0.75	ns
	Transition time, RX_CTL	$t_{t(RX\_CTL)}$		0.75		0.75		0.75	ns
Switching Characteristics for RGMII[x]_TCLK - RGMII Mode (See Figure 31)									
1	Cycle time, TXC	$t_{c(TXC)}$	360	440	36	44	7.2	8.8	ns
2	Pulse duration, TXC high	$t_{w(TXCH)}$	160	240	16	24	3.6	4.4	ns
3	Pulse duration, TXC low	$t_{w(TXCL)}$	160	240	16	24	3.6	4.4	ns
4	Transition time, TXC	$t_{t(TXC)}$		0.75		0.75		0.75	ns
Switching Characteristics for RGMII[x]_TD[3:0], and RGMII[x]_TCTL - RGMII Mode (See Figure 32)									
1	TD to TXC output skew	$t_{sk(TD-TXC)}$	-0.5	0.5	-0.5	0.5	-0.5	0.5	ns
	TX_CTL to TXC output skew	$t_{sk(TX\_CTL-TXC)}$	-0.5	0.5	-0.5	0.5	-0.5	0.5	ns
2	Transition time, TD	$t_{t(TD)}$		0.75		0.75		0.75	ns
	Transition time, TX_CTL	$t_{t(TX\_CTL)}$		0.75		0.75		0.75	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Limits			Unit
		Min	Typ	Max	
Peripheral Information and Timings – Continued					
External Memory Interfaces - *General-Purpose Memory Controller (GPMC)*					
GPMC and NOR Flash Timing Conditions—Synchronous Mode (See Figure 33 through 37)					
Input Conditions					
Input signal rise time	t_R	1		5	ns
Input signal fall time	t_F	1		5	ns
Output Condition					
Output load capacitance	C_{LOAD}	3		30	pF

No	Test	Symbol	Limits				Unit
			OPP100		**OP50**		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
External Memory Interfaces – *General-Purpose Memory Controller (GPMC) - Continued*							
GPMC and NOR Flash Timing Requirements – Synchronous Modee 27/ (See Figure 33 through 37)							
F12	Setup time, input data gpmc_ad[15:0] valid before output clock gpmc_clk high	$t_{su(dV-clkH)}$	3.2		11.1		ns
F13	Hold time, input data gpmc_ad[15:0] valid after output clock gpmc_clk high	$t_{h(clkH-dV)}$	4.74		4.74		ns
F21	Setup time, input wait gpmc_wait[x] 25/ valid before output clock gpmc_clk high	$t_{su(waitV-clkH)}$	3.2		3.2		ns
F22	Hold time, input wait gpmc_wait[x] 25/ valid after output clock gpmc_clk high	$t_{h(clkH-waitV)}$	4.74		4.74		ns
F0	Frequency 40/, output clock gpmc_clk	$1 / t_{c(clk)}$		100		50	MHz
F1	Typical pulse duration, output clock gpmc_clk high	$t_{w(clkH)}$	0.5P 37/	0.5P 37/	0.5P 37/	0.5P 37/	ns
F1	Typical pulse duration, output clock gpmc_clk low	$t_{w(clkL)}$	0.5P 37/	0.5P 37/	0.5P 37/	0.5P 37/	ns
	Duty cycle error, output clock gpmc_clk	tdc(clk)	-500	500	-500	500	ps
	Jitter standard deviation 30/, output clock gpmc_clk	tJ(clk)		33.33		33.33	ps
	Rise time, output clock gpmc_clk	tR(clk)		2		2	ns
	Fall time, output clock gpmc_clk	tF(clk)		2		2	ns
	Rise time, output data gpmc_ad[15:0]	tR(do)		2		2	ns
	Fall time, output data gpmc_ad[15:0]	tF(do)		2		2	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test		Symbol	Limits				Unit
				OPP100		OP50		
				Min	Max	Min	Max	
Peripheral Information and Timings – Continued								
External Memory Interfaces - *General-Purpose Memory Controller (GPMC) - Continued*								
GPMC and NOR Flash Switching Characteristics – Synchronous Mode - Continued 27/ (See Figure 33 through 37)								
F2	Delay time, output clock gpmc_clk rising edge to output chip select gpmc_csn[x] 26/ transition		$t_{d(clkH-csnV)}$	F – 2.2 31/	F + 4.5 31/	F – 3.2 31/	F + 9.5 31/	ns
F3	Delay time, output clock gpmc_clk rising edge to output chip select gpmc_csn[x] 26/ invalid		$t_{d(clkH-csnIV)}$	E – 2.2 30/	E + 4.5 30/	E – 3.2 30/	E + 9.5 30/	ns
F4	Delay time, output address gpmc_a[27:1] valid to output clock gpmc_clk first edge		$t_{d(aV-clk)}$	B – 4.5 27/	B + 2.3 27/	B – 5.5 27/	B + 12.3 27/	ns
F5	Delay time, output clock gpmc_clk rising edge to output address gpmc_a[27:1] invalid		$t_{d(clkH-aIV)}$	-2.3	4.5	-3.3	14.5	ns
F6	Delay time, output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n valid to output clock gpmc_clk first edge		$t_{d(be[x]nV-clk)}$	B – 1.9 27/	B + 2.3 27/	B – 2.9 27/	B + 12.3 27/	ns
F7	Delay time, output clock gpmc_clk rising edge to output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n invalid		$t_{d(clkH-be[x]nIV)}$	D – 2.3 29/	D + 1.9 29/	D – 3.3 29/	D + 11.9 29/	ns
F8	Delay time, output clock gpmc_clk rising edge to output address valid and address latch enable gpmc_advn_ale transition		$t_{d(clkH-advn)}$	G – 2.3 32/	G + 4.5 32/	G – 3.3 32/	G + 9.5 32/	ns
F9	Delay time, output clock gpmc_clk rising edge to output address valid and address latch enable gpmc_advn_ale invalid		$t_{d(clkH-advnIV)}$	D – 2.3 29/	D + 3.5 29/	D – 3.3 29/	D + 9.5 29/	ns
F10	Delay time, output clock gpmc_clk rising edge to output enable gpmc_oen transition		$t_{d(clkH-oen)}$	H – 2.3 33/	H + 3.5 33/	H – 3.3 33/	H + 8.5 33/	ns
F11	Delay time, output clock gpmc_clk rising edge to output enable gpmc_oen invalid		$t_{d(clkH-oenIV)}$	E– 2.3 33/	E + 3.5 33/	E – 3.3 33/	E + 8.5 33/	ns
F14	Delay time, output clock gpmc_clk rising edge to output write enable gpmc_wen transition		$t_{d(clkH-wen)}$	I – 2.3 34/	I + 4.5 34/	I – 3.3 34/	I + 9.5 34/	ns
F15	Delay time, output clock gpmc_clk rising edge to output data gpmc_ad[15:0] transition		$t_{d(clkH-do)}$	J – 2.3 25/	J + 1.9 25/	J – 3.3 25/	J + 11.9 25/	ns
F17	Delay time, output clock gpmc_clk rising edge to output lower byte enable and command latch enable gpmc_be0n_cle transition		$t_{d(clkH-be[x]n)}$	J – 2.3 25/	J + 1.9 25/	J – 3.3 25/	J + 11.9 25/	ns
F18	Pulse duration, output chip selectgpmc_csn[x] 26/ low	Read	$t_{w(csnV)}$	A 26/		A 26/		ns
		Write		A 26/		A 26/		ns
F19	Pulse duration, output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n low	Read	$t_{w(be[x]nV)}$	C 28/		C 28/		ns
		Write		C 28/		C 28/		ns
F20	Pulse duration, output address valid and address latch enable gpmc_advn_ale low	Read	$t_{w(advnV)}$	K 38/		K 38/		ns
		Write		K 38/		K 38/		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Limits			Unit
		Min	Typ	Max	
Peripheral Information and Timings – Continued					
External Memory Interfaces - *General-Purpose Memory Controller (GPMC)*					
GPMC and NOR Flash Timing Conditions—Asynchronous Mode (See figure 38 through 43)					
Input Conditions					
Input signal rise time	t_R	1		5	ns
Input signal fall time	t_F	1		5	ns
Output Condition					
Output load capacitance	C_{LOAD}	3		30	pF

No	Test	Limits				Unit
		OPP100		OPP50		
		Min	Max	Min	Max	
GPMC and NOR Flash Internal Timing Parameters—Asynchronous Mode – Continued. 42/ 43/ (See Figure 38 through 43)						
FI1	Delay time, output data gpmc_ad[15:0] generation from internal functional clock GPMC_FCLK 44/		6.5		6.5	ns
FI2	Delay time, input data gpmc_ad[15:0] capture from internal functional clock GPMC_FCLK 44/		4		4	ns
FI3	Delay time, output chip select gpmc_csn[x] generation from internal functional clock GPMC_FCLK 44/		6.5		6.5	ns
FI4	Delay time, output address gpmc_a[27:1] generation from internal functional clock GPMC_FCLK 44/		6.5		6.5	ns
FI5	Delay time, output address gpmc_a[27:1] valid from internal functional clock GPMC_FCLK 44/		6.5		6.5	ns
FI6	Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n generation from internal functional clock GPMC_FCLK 44/		6.5		6.5	ns
FI7	Delay time, output enable gpmc_oen generation from internal functional clock GPMC_FCLK 44/		6.5		6.5	ns
FI8	Delay time, output write enable gpmc_wen generation from internal functional clock GPMC_FCLK 44/		6.5		6.5	ns
FI9	Skew, internal functional clock GPMC_FCLK 44/		100		100	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			OPP100		OPP50		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
External Memory Interfaces - *General-Purpose Memory Controller (GPMC)*							
GPMC and NOR Flash Timing Requirements—Asynchronous Mode - Continued. (See Figure 38 through 43)							
FA5 45/	Data access time	$t_{acc(d)}$		H 49/		H 49/	ns
FA20 46/	Page mode successive data access time	$t_{acc1-pgmode(d)}$		P 48/		P 48/	ns
FA21 47/	Page mode first data access time	$t_{acc2-pgmode(d)}$		H 49/		H 49/	ns

See footnote at end of table.

No	Test		Symbol	Limits				Unit
				OPP100		OPP50		
				Min	Max	Min	Max	
GPMC and NOR Flash Switching Characteristics—Asynchronous Mode – Continued (See Figure 38 through 43)								
	Rise time, output data gpmc_ad[15:0]		$t_{R(d)}$		2		2	ns
	Fall time, output data gpmc_ad[15:0]		$t_{F(d)}$		2		2	ns
FA0	Pulse duration, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n valid time	Read	$t_{w(be[x]nV)}$		N 62/		N 62/	ns
		Write			N 62/		N 62/	ns
FA1	Pulse duration, output chip select gpmc_csn[x] 63/ low	Read	$t_{w(csnV)}$		A 51/		A 51/	ns
		Write			A 51/		A 51/	ns
FA3	Delay time, output chip select gpmc_csn[x] 63/ valid to output address valid and address latch enable gpmc_advn_ale invalid	Read	$t_{d(csnV-advnlV)}$	B – 0.2 52/	B + 2.0 52/	B – 5 52/	B + 5 52/	ns
		Write		B – 0.2 52/	B + 2.0 52/	B – 5 52/	B + 5 52/	ns
FA4	Delay time, output chip select gpmc_csn[x] 63/ valid to output enable gpmc_oen invalid (Single read)		$t_{d(csnV-oenlV)}$	C – 0.2 53/	C + 2.0 53/	C – 5 53/	C + 5 53/	ns
FA9	Delay time, output address gpmc_a[27:1] valid to output chip select gpmc_csn[x] 63/ valid		$t_{d(aV-csnV)}$	J – 0.2 59/	J + 2.0 59/	J – 5 59/	J + 5 59/	ns
FA10	Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n valid to output chip select gpmc_csn[x] 63/ valid		$t_{d(be[x]nV-csnV)}$	J – 0.2 59/	J + 2.0 59/	J – 5 59/	J + 5 59/	ns
FA12	Delay time, output chip select gpmc_csn[x] 63/ valid to output address valid and address latch enable gpmc_advn_ale valid		$t_{d(csnV-advnV)}$	K – 0.2 60/	K + 2.0 60/	K – 5 60/	K + 5 60/	ns

See footnote at end of table.

No	Test	Symbol	Limits				Unit
			OPP100		OPP50		
			Min	Max	Min	Max	

Peripheral Information and Timings – Continued

External Memory Interfaces - *General-Purpose Memory Controller (GPMC)*

GPMC and NOR Flash Switching Characteristics—Asynchronous Mode (See Figure 38 through 43)

FA13	Delay time, output chip select gpmc_csn[x] 63/ valid to output enable gpmc_oen valid	$t_{d(csnV-oenV)}$	L – 0.2 61/	L + 2.0 61/	L – 5 61/	L + 5 61/	ns
FA16	Pulse durationm output address gpmc_a[26:1] invalid between 2 successive read and write accesses	$t_{w(aIV)}$	G 57/		G 57/		ns
FA18	Delay time, output chip select gpmc_csn[x] 63/ valid to output enable gpmc_oen invalid (Burst read)	$t_{d(csnV-oenIV)}$	I – 0.2 58/	I + 2.0 58/	L – 5 58/	L + 5 58/	ns
FA20	Pulse duration, output address gpmc_a[27:1] valid - 2nd, 3rd, and 4th accesses	$t_{w(aV)}$	G 57/		G 57/		ns
FA25	Delay time, output chip select gpmc_csn[x] 63/ valid to output write enable gpmc_wen valid	$t_{d(csnV-wenV)}$	E – 0.2 55/	E + 2.0 55/	E – 5 55/	E + 5 55/	ns
FA27	Delay time, output chip select gpmc_csn[x] 63/ valid to output write enable gpmc_wen invalid	$t_{d(csnV-wenIV)}$	F – 0.2 58/	F + 2.0 58/	F– 5 58/	F + 5 58/	ns
FA28	Delay time, output write enable gpmc_ wen valid to output data gpmc_ad[15:0] valid	$t_{d(wenV-dV)}$		2.0		5	ns
FA29	Delay time, output data gpmc_ad[15:0] valid to output chip select gpmc_csn[x] 63/ valid	$t_{d(dV-csnV)}$	J – 0.2 59/	J + 2.0 59/	J – 5 59/	J + 5 59/	ns
FA37	Delay time, output enable gpmc_oen valid to output address gpmc_ad[15:0] phase end	$t_{d(oenV-aIV)}$		2.0		5	ns

See footnote at end of table.

Test	Symbol	Limits			Unit
		Min	Typ	Max	

Peripheral Information and Timings – Continued

External Memory Interfaces - *General-Purpose Memory Controller (GPMC)*

GPMC and NAND Flash—Asynchronous Mode

GPMC and NAND Flash Timing Conditions—Asynchronous Mode (See Figure 44 through 47)

Input Conditions					
Input signal rise time	t_R	1		5	ns
Input signal fall time	t_F	1		5	ns
Output Condition					
Output load capacitance	C_{LOAD}	3		30	pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits				Unit
		OPP100		OPP50		
		Min	Max	Min	Max	
Peripheral Information and Timings – Continued						
External Memory Interfaces - *General-Purpose Memory Controller (GPMC)*						
GPMC and NAND Flash—Asynchronous Mode						
GPMC and NAND Flash Internal Timing Parameters—Asynchronous Mode 64/ 65/ (See Figure 44 through 47)						
GNFI1	Delay time, output data gpmc_ad[15:0] generation from internal functional clock GPMC_FCLK) 50/		6.5		6.5	ns
GNFI2	Delay time, input data gpmc_ad[15:0] capture from internal functional clock GPMC_FCLK 50/		4.0		4.0	ns
GNFI3	Delay time, output chip select gpmc_csn[x] generation from interna functional clock GPMC_FCL 50/		6.5		6.5	ns
GNFI4	Delay time, output address valid and address latch enable gpmc_advn_ale generation from internal functional clock GPMC_FCLK 50/		6.5		6.5	ns
GNFI5	Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle generation from internal functional clock GPMC_FCLK 50/		6.5		6.5	ns
GNFI6	Delay time, output enable gpmc_oen generation from internal functional clock GPMC_FCLK 50/		6.5		6.5	ns
GNFI7	Delay time, output write enable gpmc_wen generation from internal functional clock GPMC_FCLK 50/		6.5		6.5	ns
GNFI8	Skew, functional clock GPMC_FCLK 50/		100		100	ps

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			OPP100		OPP50		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
External Memory Interfaces –*General-Purpose Memory Controller (GPMC)*							
GPMC and NAND Flash—Asynchronous Mode							
GPMC and NAND Flash Timing Requirements—Asynchronous Mode (See Figure 44 through 47)							
GNF12 66/	Access time, input data gpmc_ad[15:0]	$t_{acc(d)}$		J 67/		J 67/	ns
GPMC and NAND Flash Switching Characteristics— Asynchronous Mode (See Figure 44 through 47)							
	Rise time, output data gpmc_ad[15:0]	$t_{R(d)}$		2		2	ns
	Fall time, output data gpmc_ad[15:0]	$t_{F(d)}$		2		2	ns
GNF0	Pulse duration, output write enable gpmc_wen valid	$t_{w(wenV)}$	A 68/		A 68/		ns
GNF1	Delay time, output chip select gpmc_csn[x] 80/ valid to output write enable gpmc_wen valid	$t_{d(csnV-wenV)}$	B – 0.2 69/	B + 2.0 69/	B – 5 69/	B + 5 69/	ns
GNF2	Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle high to output write enable gpmc_wen valid	$t_{w(cleH-wenV)}$	C – 0.2 70/	C + 2.0 70/	C – 5 70/	C + 5 70/	ns
GNF3	Delay time, output data gpmc_ad[15:0] valid to output write enable gpmc_wen valid	$t_{w(wenV-dV)}$	D – 0.2 71/	D + 2.0 71/	D – 5 71/	D + 5 71/	ns
GNF4	Delay time, output write enable gpmc_wen Delay time, output write enable gpmc_wen	$t_{w(wenIV-dIV)}$	E – 0.2 72/	E + 2.0 72/	E – 5 72/	E + 5 72/	ns
GNF5	Delay time, output write enable gpmc_wen invalid to output lower-byte enable and command latch enable gpmc_be0n_cle invalid	$t_{w(wenIV-cleIV)}$	F – 0.2 73/	F + 2.0 73/	F – 5 73/	F + 5 73/	ns
GNF6	Delay time, output write enable gpmc_wen invalid to output chip select gpmc_csn[x] 80/ invalid	$t_{w(wenIV-csnIV)}$	G – 0.2 74/	G + 2.0 74/	G – 5 74/	G + 5 74/	ns
GNF7	Delay time, output address valid and address latch enable gpmc_advn_ale high to output write enable gpmc_wen valid	$t_{w(aleH-wenV)}$	C – 0.2 70/	C + 2.0 70/	C – 5 70/	C + 5 70/	ns
GNF8	Delay time, output write enable gpmc_we invalid to output address valid and address latchenable gpmc_advn_ale invalid	$t_{w(wenIV-aleIV)}$	F – 0.2 73/	F + 2.0 73/	F – 5 73/	F + 5 73/	ns
GNF9	Cycle time, write	$t_{c(wen)}$		H 75/		H 75/	
GNF10	Delay time, output chip select gpmc_csn[x] 80/ valid to output enable gpmc_oen valid	$t_{d(csnV-oenV)}$	I – 0.2 76/	I + 2.0 76/	I – 5 76/	I + 5 76/	ns
GNF13	Pulse duration, output enable gpmc_oen valid	$t_{w(oenV)}$		K 77/		K 77/	ns
GNF14	Cycle time, read	$t_{c(oen)}$	L 78/		L 78/		ns
GNF15	Delay time, output enable gpmc_oen invalid to output chip select gpmc_csn[x] 80/ invalid	$t_{w(oenIV-csnIV)}$	M– 0.2 79/	M + 2.0 79/	M – 5 79/	M + 5 79/	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test		Limits			Unit
			Min	Typ	Max	
Peripheral Information and Timings – Continued						
External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*						
mDDR (LPDDR) Routing Guidelines						
Switching Characteristics for LPDDR Memory Interface (See Figure 48)						
1	$t_{c(DDR\_CK)}$ $t_{c(DDR\_CKn)}$	Cycle time, DDR_CK and DDR_CKn	5		148/	ns
Compatible JEDEC LPDDR Devices (Per Interface) 81/						
1	JEDEC LPDDR device speed grade		LPDDR400			
2	2 JEDEC LPDDR device bit width		X16		X16	Bits
3	JEDEC LPDDR device count				1	Devices
4	JEDEC LPDDR device terminal count				60	Terminals
PCB Stackup Specifications 82/						
1	PCB routing and plane layers		4			
2	Signal routing layers		2			
3	Full ground layers under LPDDR routing region		1			
4	Number of ground plane cuts allowed within LPDDR routing region				0	
5	Full VDDS_DDR power reference layers under LPDDR routing region		1			
6	Number of layers between LPDDR routing layer and reference ground plane				0	
7	PCB routing feature size			4		mils
8	PCB trace width, w			4		mils
9	PCB BGA escape via pad size 83/			18	20	mils
10	PCB BGA escape via hole size 83/			10		mils
11	Single-ended impedance, Zo 84/			50	75	Ω
12	Impedance control 85/ 86/		Zo - 5	Zo	Zo + 5	Ω
Placement Specifications (See Figure 49) 87/						
1	X 88/ 89/				1750	mils
2	Y 88/ 89/				1280	mils
3	Y Offset 88/ 89/ 90/				650	mils
4	Clearance from non-LPDDR signal to LPDDR keepout region 91/ 92/		4			w
Bulk Bypass Capacitor 93/						
1	AM3358-EP VDDS_DDR bulk bypass capacitor count		1			Devices
2	AM3358-EP VDDS_DDR bulk bypass total capacitance		10			µF
3	DDR#1 bulk bypass capacitor count		1			Devices
4	LPDDR#1 bulk bypass total capacitance		10			µF
5	LPDDR#2 bulk bypass capacitor count 94/		1			Devices
6	LPDDR#2 bulk bypass total capacitance 94/		10			µF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits			Unit
		Min	Typ	Max	
	Peripheral Information and Timings – Continued				
	External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*				
	mDDR (LPDDR) Routing Guidelines				
	High-Speed Bypass Capacitors				
1	HS bypass capacitor package size 95/			0402	10 mils
2	Distance from HS bypass capacitor to device being bypassed			250	mils
3	Number of connection vias for each HS bypass capacitor 96/	2			Vias
4	Trace length from bypass capacitor contact to connection via			30	mils
5	Number of connection vias for each AM3358-EP VDDS_DDR and VSS terminal	1			Vias
6	Trace length from AM3358-EP VDDS_DDR and VSS terminal to connection via			35	mils
7	Number of connection vias for each LPDDR device power and ground terminal	1			Vias
8	Trace length from LPDDR device power and ground terminal to connection via			35	mils
9	AM3358-EP VDDS_DDR HS bypass capacitor count 97/	10			Devices
10	AM3358-EP VDDS_DDR HS bypass capacitor total capacitance	0.6			µF
11	LPDDR device HS bypass capacitor count 97/ 98/	8			Devices
12	LPDDR device HS bypass capacitor total capacitance 98/	0.4			µF
	LPDDR Signal Terminations				
1	CK net class 99/	0	22	Zo 100/	Ω
2	ADDR_CTRL net class 99/ 101/ 102/	0	22	Zo 100/	Ω
3	DQS0, DQS1, DQ0, and DQ1 net classes	0	22	Zo 100/	Ω
	CK and ADDR_CTRL Routing Specification 103/ 104/ **(See Figure 50)**				
1	Center-to-center CK spacing			2w	
2	CK differential pair skew length mismatch 104/ 105/			25	mils
3	CK B-to-CK C skew length mismatch			25	mils
4	Center-to-center CK to other LPDDR trace spacing 106/	4w			
5	CK and ADDR_CTRL nominal trace length 107/	CACLM - 50	CACLM	CACLM+- 50	mils
6	ADDR_CTRL-to-CK skew length mismatch			100	mils
7	ADDR_CTRL-to-ADDR_CTRL skew length mismatch			100	mils
8	Center-to-center ADDR_CTRL to other LPDDR trace spacing 106/	4w			
9	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing 106/	3w			
10	ADDR_CTRL A-to-B and ADDR_CTRL A-to-C skew length mismatch 104/			100	mils
11	ADDR_CTRL B-to-C skew length mismatch			100	mils

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits			Unit
		Min	Typ	Max	
	Peripheral Information and Timings – Continued				
	External Memory Interfaces – ***mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface***				
	mDDR (LPDDR) Routing Guidelines				
	DQS[x] and DQ[x] Routing Specification 108/ **(See Figure 51)**				
1	Center-to-center DQS[x] spacing			2w	
2	Center-to-center DDR_DQS[x] to other LPDDR trace spacing 109/	4w			
3	DQS[x] and DQ[x] nominal trace length 110/	DQLM – 50		DQLM - 50	mils
4	DQ[x]-to-DQS[x] skew length mismatch 110/			100	mils
5	DQ[x]-to-DQ[x] skew length mismatch 110/			100	mils
6	Center-to-center DQ[x] to other LPDDR trace spacing 109/ 111/	4w			
7	Center-to-center DQ[x] to other DQ[x] trace spacing 109/ 112/	3w			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits			Unit
		Min	Typ	Max	
	Peripheral Information and Timings – Continued				
	External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*				
	DDR2 Routing Guidelines				
	Switching Characteristics for DDR2 Memory Interface (See Figure 52)				
1	Cycle time, DDR_CK and DDR_CKn $t_{c(DDR\_CK)}$ $t_{c(DDR\_CKn)}$			8 113/	ns
	Compatible JEDEC DDR2 Devices (Per Interface) 114/				
1	JEDEC DDR2 device speed grade 115/	DDR2-533			
2	JEDEC DDR2 device bit width	x8		X16	bits
3	JEDEC DDR2 device count	1		2	devices
4	JEDEC DDR2 device terminal count 116/		60	84	terminals
	PCB Stackup Specifications 117/				
1	PCB routing and plane layers	4			
2	Signal routing layers	2			
3	Full ground layers under DDR2 routing region	1			
4	Number of ground plane cuts allowed within DDR2 routing region			0	
5	Full VDDS_DDR power reference layers under DDR2 routing region	1			
6	Number of layers between DDR2 routing layer and reference ground plane			0	
7	PCB routing feature size		4		mils
8	PCB trace width, w		4		mils
9	PCB BGA escape via pad size 118/		18	20	mils
10	PCB BGA escape via hole size 118/		10		mils
11	Single-ended impedance, Zo 119/		50	75	Ω
12	Impedance control 120/ 121/	Zo - 5	Zo	Zo + 5	Ω
	Placement Specifications 122/ **(See Figure 53)**				
1	X 123/ 124/			1750	mils
2	Y 123/ 124/			1280	mils
3	Y Offset 123/ 124/ 125/			650	mils
4	Clearance from non-DDR2 signal to DDR2 keepout region 126/ 127/	4			w
	Bulk Bypass Capacitors 128/				
1	AM3358-EP VDDS_DDR bulk bypass capacitor count	1			Devices
2	AM3358-EP VDDS_DDR bulk bypass total capacitance	10			µF
3	DDR2 number 1 bulk bypass capacitor count	1			Devices
4	DDR2 number 1 bulk bypass total capacitance	10			µF
5	DDR2 number 2 bulk bypass capacitor count 129/	1			Devices
6	DDR2 number 2 bulk bypass total capacitance 129/	10			µF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits			Unit
		Min	Typ	Max	
	Peripheral Information and Timings – Continued				
	External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*				
	DDR2 Routing Guideline				
	HS Bypass Capacitors				
1	HS bypass capacitor package size 130/			0402	10 mils
2	Distance from HS bypass capacitor to device being bypassed			250	mils
3	Number of connection vias for each HS bypass capacitor 131/	2			Vias
4	Trace length from bypass capacitor contact to connection via			30	mils
5	Number of connection vias for each AM3358-EP VDDS_DDR and VSS terminal	1			Vias
6	Trace length from AM3358-EP VDDS_DDR and VSS terminal to connection via			35	mils
7	Number of connection vias for each DDR2 device power and ground terminal	1			Vias
8	Trace length from DDR2 device power and ground terminal to connection via			35	mils
9	AM3358-EP VDDS_DDR HS bypass capacitor count 132/	10			Devices
10	AM3358-EP VDDS_DDR HS bypass capacitor total capacitance	0.6			µF
11	DDR2 device HS bypass capacitor count 132/ 133/	8			Devices
12	DDR2 device HS bypass capacitor total capacitance 133/	0.4			µF
	DDR2 Signal Terminations				
1	CK net class 134/	0		10	Ω
2	ADDR_CTRL net class 134/ 135/ 136/	0	22	Zo 137/	Ω
3	DQS0, DQS1, DQ0, and DQ1 net classes 138/	N/A		N/A	Ω
	Lower-Frequency DDR2 Signal Terminations				
1	CK net class 134/	0	22	Zo 137/	Ω
2	ADDR_CTRL net class 134/ 135/ 136/	0	22	Zo 137/	Ω
3	DQS0, DQS1, DQ0, and DQ1 net classes	0	22	Zo 137/	Ω
	CK and ADDR_CTRL Routing Specification 139/ 140/ **(See Figure 54)**				
1	Center-to-center CK spacing			2w	
2	CK differential pair skew length mismatch 140/ 141/			25	mils
3	CK B-to-CK C skew length mismatch			25	mils
4	Center-to-center CK to other DDR2 trace spacing 142/	4w			
5	CK and ADDR_CTRL nominal trace length 143/	CACLM - 50	CACLM	CACLM+- 50	mils
6	ADDR_CTRL-to-CK skew length mismatch			100	mils
7	ADDR_CTRL-to-ADDR_CTRL skew length mismatch			100	mils
8	Center-to-center ADDR_CTRL to other DDR2 trace spacing 142/	4w			
9	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing 142/	3w			
10	ADDR_CTRL A-to-B and ADDR_CTRL A-to-C skew length mismatch 140/			100	mils
11	ADDR_CTRL B-to-C skew length mismatch			100	mils

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits			Unit
		Min	Typ	Max	
	Peripheral Information and Timings – Continued				
	External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*				
	DDR2 Routing Guidelines				
	DQS[x] and DQ[x] Routing Specification 144/ **(See Figure 55)**				
1	Center-to-center DQS[x] spacing			2w	
2	DQS[x] differential pair skew length mismatch 141/			25	mils
3	Center-to-center DDR_DQS[x] to other LPDDR trace spacing 142/	4w			
4	DQS[x] and DQ[x] nominal trace length 145/	DQLM – 50		DQLM - 50	mils
5	DQ[x]-to-DQS[x] skew length mismatch 145/			100	mils
6	DQ[x]-to-DQ[x] skew length mismatch 145/			100	mils
7	Center-to-center DQ[x] to other LPDDR trace spacing 142/ 146/	4w			
8	Center-to-center DQ[x] to other DQ[x] trace spacing 142/ 147/	3w			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test		Limits			Unit
			Min	Typ	Max	
Peripheral Information and Timings – Continued						
External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*						
DDR3 and DDR3L Routing Guidelines						
Switching Characteristics for DDR3 Memory Interface (See fFgure 56)						
1	$t_{c(DDR\_CK)}$ $t_{c(DDR\_CKn)}$	Cycle time, DDR_CK and DDR_CKn	2.5		3.3 149/	ns
Compatible JEDEC DDR3 Devices (Per Interface)						
1	JEDEC DDR3 device speed grade	Test conditions				
		$t_{C(DDR\_CK)}$ and $t_{C(DDR\_CKn)}$ = 3.3 ns	DDR3-800			
		$t_{C(DDR\_CK)}$ and $t_{C(DDR\_CKn)}$= 2.5 ns	DDR3-1600			
2	JEDEC DDR3 device bit width		X8		X16	bits
3	JEDEC DDR3 device count 150/		1		2	devices
PCB Stackup Specifications 151/						
1	PCB routing and plane layers		4			
2	Signal routing layers		2			
3	Full ground layers under DDR3 routing region 152/		1			
4	Full VDDS_DDR power reference layers under DDR3 routing region 152/		1			
5	Number of reference plane cuts allowed within DDR3 routing region 153/				0	
6	Number of layers between DDR3 routing layer and reference plane 154/				0	
7	PCB routing feature size			4		mils
8	PCB trace width, w			4		mils
9	PCB BGA escape via pad size 155/			18	20	mils
10	PCB BGA escape via hole size /			10		mils
11	Single-ended impedance, Zo 156/			50	75	Ω
12	Impedance control 157/ 158/		Zo - 5	Zo	Zo + 5	Ω
Placement Specifications 159/ **(See Figure 57)**						
1	X 160/ 161/ 162/				1000	mils
2	Y 160/ 161/				600	mils
3	Y Offset 160/ 161/ 162/				1500	mils
4	Clearance from non-LPDDR signal to DDR3 keepout region 163/ 164/		4			w

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits			Unit
		Min	Typ	Max	
	Peripheral Information and Timings – Continued				
	External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*				
	DDR3 and DDR3L Routing Guidelines				
	Bulk Bypass Capacitors 165/				
1	AM3358-EP VDDS_DDR bulk bypass capacitor count	2			Devices
2	AM3358-EP VDDS_DDR bulk bypass total capacitance	20			µF
3	DDR3 number 1 bulk bypass capacitor count	2			Devices
4	DDR3 number 1 bulk bypass total capacitance	20			µF
5	DDR3 number 2 bulk bypass capacitor count 166/	2			Devices
6	DDR3 number 2 bulk bypass total capacitance 166/	20			µF
	High-Speed Bypass Capacitor				
1	HS bypass capacitor package size 167/		0201	0402	10 mils
2	Distance, HS bypass capacitor to AM3358-EP VDDS_DDR and VSS terminal being bypassed 168/ 169/ 170/			400	mils
3	AM3358-EP VDDS_DDR HS bypass capacitor count	20			Devices
4	AM3358-EP VDDS_DDR HS bypass capacitor total capacitance	1			µF
5	Trace length from AM3358-EP VDDS_DDR and VSS terminal to connection via 168/		35	70	mils
6	Distance, HS bypass capacitor to DDR3 device being bypassed 171/			150	mils
7	DDR3 device HS bypass capacitor count 172/	12			Devices
8	DDR3 device HS bypass capacitor total capacitance 172/	0.85			µF
9	Number of connection vias for each HS bypass capacitor 173/ 174/	2			vias
10	Trace length from bypass capacitor connect to connection via 168/ 174/		35	100	mils
11	Number of connection vias for each DDR3 device power and ground terminal 175/	1			vias
12	Trace length from DDR3 device power and ground terminal to connection via 168/ 173/		35	60	mils
	CK and ADDR_CTRL Routing Specification 176/ 177/ 178/				
1	A1 + A2 length			2500	mils
2	A1 + A2 skew			25	mils
3	A3 length			660	mils
4	A3 skew 179/			25	mils
5	A3 skew 180/			125	mils
6	AS length			100	mils

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Limits			Unit
		Min	Typ	Max	
	Peripheral Information and Timings – Continued				
	External Memory Interfaces – *mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface*				
	DDR3 and DDR3L Routing Guidelines				
	CK and ADDR_CTRL Routing Specification - Continued 176/ 177/ 178/				
7	AS skew			25	mils
8	AS+ and AS– length			70	mils
9	AS+ and AS– skew			5	mils
10	AT length 181/		500		mils
11	AT skew 182/		100		mils
12	AT skew 183/			5	mils
13	CK and ADDR_CTRL nominal trace length 184/	CACLM-50	CACLM	CACLM+50	mils
14	Center-to-center CK to other DDR3 trace spacing 185/	4w			
15	Center-to-center ADDR_CTRL to other DDR3 trace spacing 185/ 186/	4w			
16	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing 185/	3w			
17	CK center-to-center spacing 187/				
18	CK spacing to other net 185/	4w			
19	Rcp 188/	Zo - 1	Zo	Zo + 1	Ω
20	Rtt 188/ 189/	Zo - 5	Zo	Zo + 5	Ω
	DQS[x] and DQ[x] Routing Specification 190/ 191/				
1	DQ0 nominal length 192/ 193/			DQLM0	mils
2	DQ1 nominal length 192/ 194/			DQLM1	mils
3	DQ[x] skew 195/			25	mils
4	DQS[x] skew			5	mils
5	DQS[x]-to-DQ[x] skew 195/ 196/			25	mils
6	Center-to-center DQ[x] to other DDR3 trace spacing 197/ 198/	4w			
7	Center-to-center DQ[x] to other DQ[x] trace spacing 197/ 199/	3w			
8	DQS[x] center-to-center spacing 200/				
9	DQS[x] center-to-center spacing to other net 197/	4w			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			STANDARD MODE		FAST MODE		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
I²C - I²C Electrical Data and Timing							
I²C Timing Conditions – Slave Mode (See Figure 60)							
Output Condition							
	Capacitive load for each bus line			400		400	pF
Timing Requirements for I²C Input Timings (See Figure 61)							
1	Cycle time, SCL	$t_{c(SCL)}$	10		2.5		µs
2	Setup time, SCL high before SDA low (for a repeated START condition)	$t_{su(SCLH-SDAL)}$	4.7		0.6		µs
3	Hold time, SCL low after SDA low (for a START and a repeated START condition)	$t_{h(SDAL-SCLL)}$	4		0.6		µs
4	Pulse duration, SCL low	$t_{w(SCLL)}$	4.7		1.3		µs
5	Pulse duration, SCL high	$t_{w(SCLH)}$	4		0.6		µs
6	Setup time, SDA valid before SCL high	$t_{su(SDAV-SCLH)}$	250		100 201/		µs
7	Hold time, SDA valid after SCL low	$t_{h(SCLL-SDAV)}$	0 202/	3.45 203/	0 202/	0.9 203/	µs
8	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$	4.7		1.3		µs
9	Rise time, SDA	$t_{r(SDA)}$		1000		300	ns
10	Rise time, SCL	$t_{r(SCL)}$		1000		300	ns
11	Fall time, SDA	$t_{f(SDA)}$		300		300	ns
12	Fall time, SCL	$t_{f(SCL)}$		300		300	ns
13	Setup time, high before SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$	4		0.6		µs
14	Pulse duration, spike (must be suppressed)	$t_{w(SP)}$	0	50	0	50	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			STANDARD MODE		FAST MODE		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
I²C - I²C Electrical Data and Timing							
Switching Characteristics for I²C Output Timings (See Figure 61)							
15	Cycle time, SCL	$t_{c(SCL)}$	10		2.5		µs
16	Setup time, SCL high before SDA low (for a repeated ART condition)	$t_{su(SCLH-SDAL)}$	4.7		0.6		µs
17	Hold time, SCL low after SDA low (for a START and a repeated START condition)	$t_{h(SDAL-SCLL)}$	4		0.6		µs
18	Pulse duration, SCL low	$t_{w(SCLL)}$	4.7		1.3		µs
19	Pulse duration, SCL high	$t_{w(SCLH)}$	4		0.6		µs
20	Setup time, SDA valid before SCL high	$t_{su(SDAV-SCLH)}$	250		100		µs
21	Hold time, SDA valid after SCL low	$t_{h(SCLL-SDAV)}$	0	3.45	0	0.9	µs
22	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$	4.7		1.3		µs
23	Rise time, SDA	$t_{r(SDA)}$		1000		300	ns
24	Rise time, SCL	$t_{r(SCL)}$		1000		300	ns
25	Fall time, SDA	$t_{f(SDA)}$		300		300	ns
26	Fall time, SCL	$t_{f(SCL)}$		300		300	ns
27	Setup time, high before SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$	4		0.6		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			OPP100		OPP50		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
JTAG Electrical Data and Timing							
Timing Requirements for JTAG (See Figure 62)							
1	Cycle time, TCK	$t_{c(TCK)}$	81.5		104.5		ns
1a	Pulse duration, TCK high (40% of tc)	$t_{w(TCKH)}$	32.6		41.8		ns
1b	Pulse duration, TCK low (40% of tc)	$t_{w(TCKL)}$	32.6		41.8		ns
3	Input setup time, TDI valid to TCK high	$t_{su(TDI-TCKH)}$	3		3		ns
	Input setup time, TMS valid to TCK high	$t_{su(TMS-TCKH)}$	3		3		ns
4	Input hold time, TDI valid from TCK high	$t_{h(TCKH-TDI)}$	8.05		8.05		ns
	Input hold time, TMS valid from TCK high	$t_{h(TCKH-TMS)}$	8.05		8.05		ns
Switching Characteristics for JTAG (See Figure 62)							
2	Delay time, TCK low to TDO valid	$t_{d(TCKL-TDO)}$	3	27.6	4	36.8	ns

No	Test	Symbol	Limits		Unit
			Min	Max	
Peripheral Information and Timings – Continued					
LCD Controller (LCDC)					
LCD Interface Display Driver (LIDD Mode)					
LCD Controller Timing Conditions					
Output Condition					
	Output load capacitance – LIDD mode	C_{LOAD}	5	60	pF
	Output load capacitance – Raster mode	C_{LOAD}	3	30	pF

No	Test	Symbol	OPP100		Unit
			Min	Max	
Peripheral Information and Timings – Continued					
7.10 LCD Controller (LCDC)					
7.10.1 LCD Interface Display Driver (LIDD Mode)					
Timing Requirements for LCD LIDD Mode (See Figure 64 through 72)					
16	Setup time, LCD_DATA[15:0] valid before LCD_MEMORY_CLK high	$t_{su(LCD\_DATA-LCD\_MEMORY\_CLK)}$	18		ns
17	Hold time, LCD_DATA[15:0] valid after LCD_MEMORY_CLK high	$t_{h(LCD\_MEMORY\_CLK-LCD\_DATA)}$	0		ns
18	Transition time, LCD_DATA[15:0]	$t_{t(LCD\_DATA)}$	1	3	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	OPP100		Unit
			Min	Max	
Peripheral Information and Timings – Continued					
LCD Controller (LCDC)					
LCD Interface Display Driver (LIDD Mode)					
Switching Characteristics for LCD LIDD Mode (See Figure 64 through figure 72)					
1	Cycle time, LCD_MEMORY_CLK	$t_{c(LCD\_MEMORY\_CLK)}$	23.7		ns
2	Pulse duration, LCD_MEMORY_CLK high	$t_{w(LCD\_MEMORY\_CLKH)}$	0.45 tc	0.55tc	ns
3	Pulse duration, LCD_MEMORY_CLK low	$t_{w(LCD\_MEMORY\_CLKL)}$	0.45 tc	0.55tc	ns
4	Delay time, LCD_MEMORY_CLK high to LCD_DATA[15:0] valid (write)	$t_{d(LCD\_MEMORY\_CLK-LCD\_DATAV)}$		7	ns
5	Delay time, LCD_MEMORY_CLK high to LCD_DATA[15:0] invalid (write)	$td_{(LCD\_MEMORY\_CLK-LCD\_DATAI)}$	0		ns
6	Delay time, LCD_MEMORY_CLK high to LCD_AC_BIAS_EN	$t_{d(LCD\_MEMORY\_CLK-LCD\_AC\_BIAS\_EN)}$	0	6.8	ns
7	Transition time, LCD_AC_BIAS_EN	$t_{t(LCD\_AC\_BIAS\_EN)}$	1	10	ns
8	Delay time, LCD_MEMORY_CLK high to LCD_VSYNC	$t_{d(LCD\_MEMORY\_CLK-LCD\_VSYNC)}$	0	7	ns
9	Transition time, LCD_VSYNC	$t_{t(LCD\_VSYNC)}$	1	10	ns
10	Delay time, LCD_MEMORY_CLK high to LCD_HSYNC	$t_{d(LCD\_MEMORY\_CLK-LCD\_HYSNC)}$	0	7	ns
11	Transition time, LCD_HYSNC	$t_{t(LCD\_HSYNC)}$	1	10	ns
12	Delay time, LCD_MEMORY_CLK high to LCD_PCLK	$t_{d(LCD\_MEMORY\_CLK-LCD\_PCLK)}$	0	7	ns
13	Transition time, LCD_PCLK	$t_{t(LCD\_PCLK)}$	1	10	ns
14	Delay time, LCD_MEMORY_CLK high to LCD_DATA[15:0] high-Z	$t_{d(LCD\_MEMORY\_CLK-LCD\_DATAZ)}$	0	7	ns
15	Delay time, LCD_MEMORY_CLK high to LCD_DATA[15:0] driven	$t_{d(LCD\_MEMORY\_CLK-LCD\_DATA)}$	0	7	ns
19	Transition time, LCD_MEMORY_CLK	$t_{t(LCD\_MEMORY\_CLK)}$	1	2.5	ns
20	Transition time, LCD_DATA	$t_{t(LCD\_DATA)}$	1	10	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			OPP50		OPP100		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
LCD Controller (LCDC)							
LCD Raster Mode							
Switching Characteristics for LCD Raster Mode (See Figure 73 through figure 76)							
1	Cycle time, pixel clock	$t_{c(LCD\_PCLK)}$	15.8		7.9		ns
2	Pulse duration, pixel clock high	$t_{w(LCD\_PCLKH)}$	0.45 tc	0.55tc	0.45 tc	0.55tc	ns
3	Pulse duration, pixel clock low	$t_{w(LCD\_PCLKL)}$	0.45 tc	0.55tc	0.45 tc	0.55tc	ns
4	Delay time, LCD_PCLK to LCD_DATA[23:0] valid (write)	$t_{d(LCD\_PCLK-LCD\_DATAV)}$		3.0		1.9	ns
5	Delay time, LCD_PCLK to LCD_DATA[23:0] invalid (write)	$t_{d(LCD\_PCLK-LCD\_DATAI)}$	-3.0		-1.7		ns
6	Delay time, LCD_PCLK to LCD_AC_BIAS_EN	$t_{d(LCD\_PCLK-LCD\_AC\_BIAS\_EN)}$	-3.0	3.0	-1.7	1.9	ns
7	Transition time, LCD_AC_BIAS_EN	$t_{t(LCD\_AC\_BIAS\_EN)}$	0.5	2.4	0.5	2.4	ns
8	Delay time, LCD_PCLK to LCD_VSYNC	$t_{d(LCD\_PCLK-LCD\_VSYNC)}$	-3.0	3.0	-1.7	1.9	ns
9	Transition time, LCD_VSYNC	$t_{t(LCD\_VSYNC)}$	0.5	2.4	0.5	2.4	ns
10	Delay time, LCD_PCLK to LCD_HSYNC	$t_{d(LCD\_PCLK-LCD\_HSYNC)}$	-3.0	3.0	-1.7	1.9	ns
11	Transition time, LCD_HSYNC	$t_{t(LCD\_HSYNC)}$	0.5	2.4	0.5	2.4	ns
12	Transition time, LCD_PCLK	$t_{t(LCD\_PCLK)}$	0.5	2.4	0.5	2.4	ns
13	Transition time, LCD_DATA	$t_{t(LCD\_DATA)}$	0.5	2.4	0.5	2.4	ns

No	Test	Symbol	Limits			Unit
			Min	Typ	Max	
Peripheral Information and Timings – Continued						
Multichannel Audio Serial Port (McASP)						
McASP Electrical Data and Timing						
McASP Timing Conditions						
Input Conditions						
	Input signal rise time	t_R	1 204/		4 204/	ns
	Input signal fall time	t_F	1 204/		4 204/	ns
Output Condition						
	Output load capacitance	C_{LOAD}	15		30	pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test		Symbol	Limits				Unit
				OPP100		OPP50		
				Min	Max	Min	Max	
Peripheral Information and Timings – Continued								
Multichannel Audio Serial Port (McASP)								
McASP Electrical Data and Timing								
Timing Requirements for McASP 205/ **(See figure 78)**								
1	Cycle time, McASP[x]_AHCLKR and McASP[x]_AHCLKX		$t_{c(AHCLKRX)}$	20		40		ns
2	Pulse duration, McASP[x]_AHCLKR and McASP[x]_AHCLKX high or low		$t_{w(AHCLKRX)}$	0.5P – 2.5 206/		0.5P – 2.5 206/		ns
3	Cycle time, McASP[x]_ACLKR and McASP[x]_ACLKX		$t_{c(ACLKRX)}$	20		40		ns
4	Pulse duration, McASP[x]_ACLKR and McASP[x]_ACLKX high or low		$t_{w(ACLKRX)}$	0.5R – 2.5 207/		0.5R – 2.5 207/		ns
5	Setup time, McASP[x]_AFSR and McASP[x]_AFSX input valid before McASP[x]_ACLKR and McASP[x]_ACLKX	ACLKR and ACLKX int	$t_{su(AFSRX- ACLKRX)}$	11.5		15.5		ns
		ACLKR and ACLKX ext in		4		6		
		ACLKR and ACLKX ext out		4		6		
6	Hold time, McASP[x]_AFSR and McASP[x]_AFSX input valid after McASP[x]_ACLKR and McASP[x]_ACLKX	ACLKR and ACLKX int	$t_{h(ACLKRX- AFSRX)}$	-1		-1		ns
		ACLKR and ACLKX ext in		0.4		0.4		
		ACLKR and ACLKX ext out		0.4		0.4		
7	Setup time, McASP[x]_AXR input valid before McASP[x]_ACLKR and McASP[x]_ACLKX	ACLKR and ACLKX int	$t_{su(AXR-ACLKRX)}$	11.5		15.5		ns
		ACLKR and ACLKX ext in		4		6		
		ACLKR and ACLKX ext out		4		6		
8	Hold time, McASP[x]_AXR input valid after McASP[x]_ACLKR and McASP[x]_ACLKX	ACLKR and ACLKX int	$t_{h(ACLKRX-AXR)}$	-1		-1		ns
		ACLKR and ACLKX ext in		0.4		0.4		
		ACLKR and ACLKX ext out		0.4		0.4		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test		Symbol	Limits				Unit
				OPP100		OPP50		
				Min	Max	Min	Max	
Peripheral Information and Timings – Continued								
Multichannel Audio Serial Port (McASP)								
McASP Electrical Data and Timing								
Switching Characteristics for McASP 205/ **(See figure 78)**								
9	Cycle time, McASP[x]_AHCLKR and McASP[x]_AHCLKX		$t_{c(AHCLKRX)}$	20		40		ns
10	Pulse duration, McASP[x]_AHCLKR and McASP[x]_AHCLKX high or low		$t_{w(AHCLKRX)}$	0.5P – 2.5 206/		0.5P – 2.5 206/		ns
11	Cycle time, McASP[x]_ACLKR and McASP[x]_ACLKX		$t_{c(ACLKRX)}$	20		40		ns
12	Pulse duration, McASP[x]_ACLKR and McASP[x]_ACLKX high or low		$t_{w(ACLKRX)}$	0.5P – 2.5 207/		0.5P – 2.5 207/		ns
13	Delay time, McASP[x]_ACLKR and McASP[x]_ACLKX transmit edge to McASP[x]_AFSR and McASP[x]_AFSX output valid	ACLKR and ACLKX int	$t_{d(ACLKRX-AFSRX)}$	0	6	0	6	ns
		ACLKR and ACLKX ext in		2	13.5	2	18	
	Delay time, McASP[x]_ACLKR and McASP[x]_ACLKX transmit edge to McASP[x]_AFSR and McASP[x]_AFSX output valid with Pad Loopback	ACLKR and ACLKX ext out		2	13.5	2	18	
14	Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid	ACLKX in	$t_{d(ACLKX-AXR)}$	0	6	0	6	ns
		ACLKX ext in		2	13.5	2	18	
	Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid with Pad Loopback	ACLKX ext out		2	13.5	2	18	
15	Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance	ACLKX in	$t_{dis(ACLKX-AXR)}$	0	6	0	6	ns
		ACLKX ext in		2	13.5	2	18	
	Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance with pad loopback	ACLKX ext out		2	13.5	2	18	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits		Unit
			Min	Max	
Peripheral Information and Timings – Continued					
Multichannel Serial Port Interface (McSPI)					
McSPI Electrical Data and Timing					
McSPI Timing Conditions – Slave Mode					
Input Conditions					
	Input signal rise time	t_r		5	ns
	Input signal fall time	t_f		5	ns
Output Condition20					
	Output load capacitance	C_{load}		20	pF

No	Test	Symbol	Limits				Unit
			OPP100		OPP50		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
Multichannel Serial Port Interface (McSPI)							
McSPI Electrical Data and Timing							
Timing Requirements for McSPI Input Timings—Slave Mode (See Figure 79)							
1	Cycle time, SPI_CLK	$t_{c(SPICLK)}$	62.5		124.8		ns
2	Typical pulse duration, SPI_CLK low	$t_{w(SPICLKL)}$	0.5P – 3.12 208/	0.5P + 3.12 208/	0.5P – 3.12 208/	0.5P + 3.12 208/	ns
3	Typical pulse duration, SPI_CLK high	$t_{w(SPICLKH)}$	0.5P – 3.12 208/	0.5P + 3.12 208/	0.5P – 3.12 208/	0.5P + 3.12 208/	ns
4	Setup time, SPI_D[x] (SIMO) valid before SPI_CLK active edge 209/ 210/	$t_{su(SIMO-SPICLK)}$	12.92		12.92		ns
5	Hold time, SPI_D[x] (SIMO) valid after SPI_CLK active edge 209/ 210/	$t_{h(SPICLK-SIMO)}$	12.92		12.92		ns
8	Setup time, SPI_CS valid before SPI_CLK first edge 209/	$t_{su(CS-SPICLK)}$	12.92		12.92		ns
9	Hold time, SPI_CS valid after SPI_CLK last edge 209/	$t_{h(SPICLK-CS)}$	12.92		12.92		ns
Switching Characteristics for McSPI Output Timings—Slave Mode (See figure 80)							
6	Delay time, SPI_CLK active edge to SPI_D[x] (SOMI) transition 209/ 210/	$t_{d(SPICLK-SOMI)}$	-4.00	17.12	-4.00	17.12	ns
7	Delay time, SPI_CS active edge to SPI_D[x] (SOMI) transition 209/ 210/	$t_{d(CS-SOMI)}$		17.12		17.12	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	LOW LOAD		HIGH LOAD		Unit
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
Multichannel Serial Port Interface (McSPI)							
McSPI Electrical Data and Timing							
McSPI Timing Conditions – Master Mode							
Input Conditions							
	Input signal rise time	t_r		8		8	ns
	Input signal fall time	t_f		8		8	ns
Output Condition20							
	Output load capacitance	C_{load}		5		25	pF

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test		Symbol	Limits								Unit
				OPP100				OPP50				
				LOW LOAD		HIGH LOAD		LOW LOAD		HIGH LOAD		
				Min	Max	Min	Max	Min	Max	Min	Max	
Peripheral Information and Timings – Continued												
Multichannel Serial Port Interface (McSPI)												
McSPI Electrical Data and Timing												
Timing Requirements for McSPI Input Timings— Master Mode (See Figure 81)												
4	Setup time, SPI_D[x] (SOMI) valid before SPI_CLK active edge		$t_{su(SOMI-SPICLKH)}$	2.29		3.02		2.29		3.02		ns
5	Hold time, SPI_D[x] (SOMI) valid after SPI_CLK active edge		$t_{h(SPICLKH-SOMI)}$	7.25		7.25		7.7		7.7		ns
Switching Characteristics for McSPI Output Timings—Master Mode (See Figure 82)												
1	Cycle time, SPI_CLK		$t_{c(SPICLK)}$	20.8		20.8		41.6		41.6		ns
2	Typical pulse duration, SPI_CLK low		$t_{w(SPICLKL)}$	0.5P – 1.04 208/	0.5P – 1.04 208/	0.5P – 2.08 208/	0.5P – 2.08 208/	0.5P – 1.04 208/	0.5P – 1.04 208/	0.5P – 2.08 208/	0.5P – 2.08 208/	ns
3	Typical pulse duration, SPI_CLK high		$t_{w(SPICLKH)}$	0.5P – 1.04 208/	0.5P – 1.04 208/	0.5P – 2.08 208/	0.5P – 2.08 208/	0.5P – 1.04 208/	0.5P – 1.04 208/	0.5P – 2.08 208/	0.5P – 2.08 208/	ns
	Rising time, SPI_CLK		$t_{r(SPICLK)}$		3.82		3.82		3.82		3.82	ns
	Falling time, SPI_CLK		$t_{f(SPICLK)}$		3.44		3.44		3.44		3.44	ns
6	Delay time, SPI_CLK active edge to SPI_D[x] (SIMO) transition 211/		$t_{d(SPICLK-SIMO)}$	-3.57	3.57	-4.62	4.62	-3.57	3.57	-4.62	4.62	ns
7	Delay time, SPI_CS active edge to SPI_D[x] (SIMO) ransition 211/		$t_{d(CS-SIMO)}$		3.57		4.62		3.57		4.62	ns
8	Delay time, SPI_CS active to SPI_CLK first edge	Mode 1 and 3 212/	$t_{d(CS-SPICLK)}$	A – 4.2 213/		A – 2.54 213/		A – 4.2 213/		A – 2.54 213/		ns
		Mode 0 and 2 212/		B – 4.2 214/		B – 2.54 214/		B – 4.2 214/		B – 2.54 214/		ns
9	Delay time, SPI_CLK last edge to SPI_CS nactive	Mode 1 and 3 212/	$t_{d(SPICLK-CS)}$	B – 4.2 214/		B – 2.54 214/		B – 4.2 214/		B – 2.54 214/		ns
		Mode 0 and 2 212/		A – 4.2 213/		A – 2.54 213/		A – 4.2 213/		A – 2.54 213/		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits			Unit
			Min	Typ	Max	
Peripheral Information and Timings – Continued						
Multimedia Card (MMC) Interface						
MMC Electrical Data and Timing						
MMC Timing Conditions						
Input Conditions						
	Input signal rise time	t_r	1		5	ns
	Input signal fall time	t_f	1		5	ns
Output Condition						
	Output load capacitance	C_{load}	3		30	pF
Timing Requirements for MMC[x]_CMD and MMC[x]_DAT[7:0] (See Figure 83)						
1	Setup time, MMC_CMD valid before MMC_CLK rising clock edge	$t_{su(CMDV-CLKH)}$	4.1			ns
2	Hold time, MMC_CMD valid after MMC_CLK rising clock edge	$t_{h(CLKH-CMDV)}$	3.76			ns
3	Setup time, MMC_DATx valid before MMC_CLK rising clock edge	$t_{su(DATV-CLKH)}$	4.1			ns
4	Hold time, MMC_DATx valid after MMC_CLK rising clock edge	$t_{h(CLKH-DATV)}$	3.76			ns

No	Test	Symbol	Limits				Unit
			STANDARD MODE		**HIGH-SPEED MODE**		
			Min	Max	Min	Max	
Switching Characteristics for MMC[x]_CLK (See Figure 84)							
5	Operating frequency, MMC_CLK	$f$op(CLK)		24		48	MHz
	Operating period: MMC_CLK	tcop(CLK)	41.7		20.8		ns
	Identification mode frequency, MMC_CLK	fid(CLK)		400		400	kHz
	Identification mode period: MMC_CLK	tcid(CLK)	2500		2500		ns
6	Pulse duration, MMC_CLK low	tw(CLKL)	(0.5 × P) – $t_{f(CLK)}$ 215/		(0.5 × P) – $t_{f(CLK)}$ 215/		ns
7	Pulse duration, MMC_CLK high	tw(CLKH)	(0.5 × P) – $t_{f(CLK)}$ 215/		(0.5 × P) – $t_{f(CLK)}$ 215/		ns
8	Rise time, all signals (10% to 90%)	8 tr(CLK)		2.2		2.2	ns
9	Fall time, all signals (10% to 90%)	tf(CLK)		2.2		2.2	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			OPP100		OPP50		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
Multimedia Card (MMC) Interface							
MMC Electrical Data and Timing							
Switching Characteristics for MMC[x]_CMD and MMC[x]_DAT[7:0] – Standard Mode (See Figure 85)							
10	Delay time, MMC_CLK falling clock edge to MMC_CMD transition	$t_{d(CLKL-CMD)}$	-4	14	-4	17.5	ns
11	Delay time, MMC_CLK falling clock edge to MMC_DATx transition	$t_{d(CLKL-DAT)}$	-4	14	-4	17.5	ns
Switching Characteristics for MMC[x]_CMD and MMC[x]_DAT[7:0]—High-Speed Mode (See Figure 86)							
12	Delay time, MMC_CLK rising clock edge to MMC_CMD transition	$t_{d(CLKL-CMD)}$	2.5	14	2.5	17.5	ns
13	Delay time, MMC_CLK rising clock edge to MMC_DATx transition	$t_{d(CLKL-DAT)}$	2.5	14	2.5	17.5	ns

No	Test		Symbol	Limits			Unit
				Min	Typ	Max	
Peripheral Information and Timings – Continued							
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)							
Programmable Real-Time Unit (PRU-ICSS PRU)							
PRU-ICSS PRU Timing Conditions							
Output Condition							
	Capacitive load for each bus line		C_{load}			30	pF
PRU-ICSS PRU Timing Requirements - Direct Input Mode (See Figure 87)							
1	Pulse width, GPI		$t_{w(GPI)}$	2 × P 216/			ns
2	Rise time, GPI		$t_{r(GPI)}$	1.0		3.9	ns
	Fall time, GPI		$t_{f(GPI)}$	1.0		3.0	ns
3	Internal skew between GPI[n:0] signals 217/	PRU0	$t_{sk(GPI)}$			1.0	ns
		PRU1				3.0	ns
PRU-ICSS PRU Switching Requirements – Direct Output Mode (See Figure 88)							
1	Pulse width, GPI		$t_{w(GPO)}$	2 × P 216/			ns
2	Rise time, GPI		$t_{r(GPO)}$	1.0		3.9	ns
	Fall time, GPI		$t_{f(GPO)}$	1.0		3.0	ns
3	Internal skew between GPI[n:0] signals 218/	PRU0	$t_{sk(GPO)}$			1.0	ns
		PRU1				5.0	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits		Unit
			Min	Max	
Peripheral Information and Timings – Continued					
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)					
PRU-ICSS PRU Parallel Capture Mode Electrical Data and Timing					
PRU-ICSS PRU Timing Requirements - Parallel Capture Mode (See Figure 89 and Figure 90)					
1	Cycle time, CLOCKIN	$t_{c(CLOCKIN)}$	20.00		ns
2	Pulse duration, CLOCKIN low	$t_{w(CLOCKIN\_L)}$	10.00		ns
3	Pulse duration, CLOCKIN high	$t_{w(CLOCKIN\_H)}$	10.00		ns
4	Rising time, CLOCKIN	$t_{r(CLOCKIN)}$	1.00	3.00	ns
5	Falling time, CLOCKIN	$t_{f(CLOCKIN)}$	1.00	3.00	ns
6	Setup time, DATAIN valid before CLOCKIN	$t_{su(DATAIN-CLOCKIN)}$	5.00		ns
7	Hold time, DATAIN valid after CLOCK	$t_{h(CLOCKIN-DATAIN)}$	0.00		ns
8	Rising time, DATAIN	$t_{r(DATAIN)}$	1.00	3.00	ns
	Falling time, DATAIN	$t_{f(DATAIN)}$	1.00	3.00	ns
7.14.1.3 PRU-ICSS PRU Shift Mode Electrical Data and Timing					
PRU-ICSS PRU Timing Requirements – Shift In Mode (See Figure 91)					
1	Cycle time, DATAIN	$t_{c(DATAIN)}$	10.00		ns
2	Pulse width, DATAIN	$t_{w(DATAIN)}$	0.45 × P 216/	0.55 × P 216/	ns
3	Rising time, DATAIN	$t_{r(DATAIN)}$	1.00	3.00	ns
4	Falling time, DATAIN	$t_{f(DATAIN)}$	1.00	3.00	ns
PRU-ICSS PRU Switching Requirements - Shift Out Mode (See Figure 92)					
1	Cycle time, CLOCKOUT	$t_{c(CLOCKOUT)}$	10.00		ns
2	Pulse width, CLOCKOUT	$t_{w(CLOCKOUT)}$	0.45 × P 216/	0.55 × P 216/	ns
3	Rising time, CLOCKOUT	$t_{r(CLOCKOUT)}$	1.00	3.00	ns
4	Falling time, CLOCKOUT	$t_{f(CLOCKOUT)}$	1.00	3.00	ns
5	Delay time, CLOCKOUT to DATAOUT valid	$t_{d(CLOCKOUT-DATAOUT)}$	0.00	3.00	ns
6	Rising time, DATAOUT	$t_{r(DATAOUT)}$	1.00	3.00	ns
	Falling time, DATAOUT	$t_{f(DATAOUT)}$	1.00	3.00	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits			Unit
			Min	Typ	Max	
Peripheral Information and Timings – Continued						
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem(PRU-ICSS)						
PRU-ICSS MII_RT and Switch						
PRU-ICSS MII_RT Switch Timing Conditions						
Input Conditions						
	Input signal rise time	t_R	1 218/		3 218/	ns
	Input signal fall time	t_F	1 218/		3 218/	ns
Output Condition						
	Output load capacitance	C_{LOAD}	3		20	pF
7.14.2.1 PRU-ICSS MDIO Electrical Data and Timing						
PRU-ICSS MDIO Timing Requirements – MDIO_DATA (See Figure 93)						
1	Setup time, MDIO valid before MDC high	$t_{su(MDIO-MDC)}$	90			ns
2	Hold time, MDIO valid from MDC high	$t_{h(MDIO-MDC)}$	0			ns
PRU-ICSS MDIO Switching Characteristics - MDIO_CLK (See Figure 94)						
1	Cycle time, MDC	$t_{c(MDC)}$	400			ns
2	Pulse duration, MDC high	$tw_{(MDCH)}$	160			ns
3	Pulse duration, MDC low	$t_{w(MDCL)}$	160			ns
4	Transition time, MDC	$t_{t(MDC)}$			5	ns
PRU-ICSS MDIO Switching Characteristics – MDIO_DATA (See Figure 95)						
1	Delay time, MDC high to MDIO valid	$t_{d(MDC-MDIO)}$	10		390	ns

No	Test	Symbol	Limits				Unit
			10 Mbps		100 Mbps		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem(PRU-ICSS)							
PRU-ICSS MII_RT and Switch							
PRU-ICSS MII_RT Electrical Data and Timing							
PRU-ICSS MII_RT Timing Requirements – MII_RXCLK (See Figure 96)							
1	Cycle time, RX_CLK	$t_{c(RX\_CLK)}$	399.96	400.04	39.996	40.004	ns
2	Pulse duration, RX_CLK high	$t_{w(RX\_CLKH)}$	140	260	14	26	ns
3	Pulse duration, RX_CLK low	$t_{w(RX\_CLKL)}$	140	260	14	26	ns
4	Transition time, RX_CLK	$t_{t(RX\_CLK)}$		3		3	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits				Unit
			10 Mbps		100 Mbps		
			Min	Max	Min	Max	
Peripheral Information and Timings – Continued							
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem(PRU-ICSS)							
PRU-ICSS MII_RT and Switch							
PRU-ICSS MII_RT Electrical Data and Timing							
PRU-ICSS MII_RT Timing Requirements – MII[x]_TXCLK (See Figure 97)							
1	Cycle time, TX_CLK	$t_{c(TX\_CLK)}$	399.96	400.04	39.996	40.004	ns
2	Pulse duration, TX_CLK high	$t_{w(TX\_CLKH)}$	140	260	14	26	ns
3	Pulse duration, TX_CLK low	$t_{w(TX\_CLKL)}$	140	260	14	26	ns
4	Transition time, TX_CLK	$t_{t(TX\_CLK)}$		3		3	ns
PRU-ICSS MII_RT Timing Requirements - MII_RXD[3:0], MII_RXDV, and MII_RXER (See Figure 98)							
1	Setup time, RXD[3:0] valid before RX_CLK	$t_{su(RXD-RX\_CLK)}$	8		8		ns
	Setup time, RX_DV valid before RX_CLK	$t_{su(RX\_DV-RX\_CLK)}$					
	Setup time, RX_ER valid before RX_CLK	$t_{su(RX\_ER-RX\_CLK)}$					
2	Hold time RXD[3:0] valid after RX_CLK	$t_{h(RX\_CLK-RXD)}$	8		8		ns
	Hold time RX_DV valid after RX_CLK	$t_{h(RX\_CLK-RX\_DV)}$					
	Hold time RX_ER valid after RX_CLK	$t_{h(RX\_CLK-RX\_ER)}$					
RU-ICSS MII_RT Switching Characteristics - MII_TXD[3:0] and MII_TXEN (See Figure 99)							
1	Delay time, TX_CLK high to TXD[3:0] valid	$t_{d(TX\_CLK-TXD)}$	5	25	5	25	ns
	Delay time, TX_CLK to TX_EN valid	$t_{d(TX\_CLK-TX\_EN)}$					

No	Test	Symbol	Limits		Unit
			Min	Max	
Peripheral Information and Timings – Continued					
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem(PRU-ICSS)					
PRU-ICSS Universal Asynchronous Receiver Transmitter (PRU-ICSS UART)					
Timing Requirements for PRU-ICSS UART Receive (See Figure 100)					
3	Pulse duration, receive start, stop, data bit	$t_{w(RX)}$	0.96U 220/	1.05U 220/	ns
Switching Characteristics Over Recommended Operating Conditions for PRU-ICSS UART Transmit					
1	Maximum programmable baud rate	$f_{baud(baud)}$	0	12	MHz
2	Pulse duration, transmit start, stop, data bit	$t_{w(TX)}$	U – 2 220/	U + 2 220/	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits		Unit
			Min	Max	
Peripheral Information and Timings – Continued					
Universal Asynchronous Receiver Transmitter (UART)					
UART Electrical Data and Timing					
Timing Requirements for UARTx (See Figure 101)					
3	Pulse duration, receive start, stop, data bit	$t_{w(RX)}$	0.96U 220/	1.05U 220/	ns
Switching Characteristics for UARTx Transmit (See Figure 101)					
1	Maximum programmable baud rate	$f_{baud(baud)}$		3.6884	MHz
2	Pulse duration, transmit start, stop, data bit	$t_{w(TX)}$	U – 2 220/	U + 2 220/	ns
UART IrDA Interface					
UART IrDA—Signaling Rate and Pulse Duration—Receive Mode (See Figure 102)					
	SIGNALING RATE		**ELECTRICAL PULSE DURATION**		
SIR					
	2.4 Kbps		1.41	88.55	µs
	9.6 Kbps		1.41	22.13	µs
	19.2 Kbps		1.41	11.07	µs
	38.4 Kbps		1.41	5.96	µs
	57.6 Kbps		1.41	4.34	µs
	115.2 Kbps		1.41	2.23	µs
MIR					
	0.576 Mbps		297.2	518.8	ns
	1.152 Mbps		149.6	258.4	ns
FIR					
	4 Mbps (single pulse)		67	164	ns
	4 Mbps (double pulse)		190	289	ns
UART IrDA—Signaling Rate and Pulse Duration—Transmit Mode					
SIR					
	2.4 Kbps		78.1	78.1	µs
	9.6 Kbps		19.5	19.5	µs
	19.2 Kbps		9.75	9.75	µs
	38.4 Kbps		4.87	4.87	µs
	57.6 Kbps		3.25	3.25	µs
	115.2 Kbps		1.62	1.62	µs
MIR					
	0.576 Mbps		414	419	ns
	1.152 Mbps		206	211	ns
FIR					
	4 Mbps (single pulse)		123	128	ns
	4 Mbps (double pulse)		248	253	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ over recommended ranges of supply voltage and operating temperature (unless otherwise noted).
3/ The interfaces or signals described in this table correspond to the interfaces or signals available in multiplexing mode 0. All interfaces or signals multiplexed on the terminals described in this table have the same dc electrical characteristics.
4/ The input voltage thresholds for this input are not a function of VDDSHV6.
5/ The typical value corresponds to 1 cap of 10 µF and 8 caps of 10 nF.
6/ The typical value corresponds to 1 cap of 10 µF and 5 caps of 10 nF.
7/ Typical values consist of 1 cap of 10 µF and 4 caps of 10 nF.
8/ For more details on decoupling capacitor requirements for the mDDR(LPDDR), DDR2, DDR3, DDR3L memory interface, see Section 7.7.2.1.2.6 and Section 7.7.2.1.2.7 from manufacturer data when using mDDR(LPDDR) memory devices, Section 7.7.2.2.2.6 and Section 7.7.2.2.2.7 from manufacturer data when using DDR2 memory devices, or Section 7.7.2.3.3.6 and Section 7.7.2.3.3.7 from manufacturer data when using DDR3 or DDR3L memory devices.
9/ VDDS_SRAM_CORE_BG supply powers an internal LDO for SRAM supplies. Inrush currents could cause voltage drop on the VDDS_SRAM_CORE_BG supplies when the SRAM LDO is enabled after powering up VDDS_SRAM_CORE_BG terminals. A 10 µF is recommended to be placed close to the terminal and routed with widest traces possible to minimize the voltage drop on VDDS_SRAM_CORE_BG terminals.
10/ VDDS_SRAM_MPU_BB supply powers an internal LDO for SRAM supplies. Inrush currents could cause voltage drop on the VDDS_SRAM_MPU_BB supplies when the SRAM LDO is enabled after powering up VDDS_SRAM_MPU_BB terminals. A 10 µF is recommended to be placed close to the terminal and routed with widest traces possible to minimize the voltage drop on VDDS_SRAM_MPU_BB terminals.
11/ Typical values consist of 1 cap of 10 µF and 2 caps of 10 nF.
12/ Typical values consist of 1 cap of 10 µF and 6 caps of 10 nF.
13/ LDO regulator outputs should not be used as a power source for any external components.
14/ The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the RTC_KLDO_ENn terminal is high.
15/ VREFP and VREFN must be tied to ground if the internal voltage reference is used.
16/ This parameter is valid when the respective AIN terminal is configured to operate as a general-purpose ADC input.
17/ Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.
18/ $Pxtal = 0.5\ ESR\ (2\ \pi\ fxtal\ CL\ VDDS\_OSC)^2$
19/ Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.
20/ $Pxtal = 0.5\ ESR\ (2\ \pi\ fxtal\ CL\ VDDS\_RTC)^2$
21/ Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.
22/ H = Period of baud rate, 1 / programmed baud rate.
23/ P = Period of PICLKOCP (interface clock).
24/ Except when specified otherwise.
25/ In gpmc_wait[x], x is equal to 0 or 1.
26/ For single read: A = (CSRdOffTime – CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst read: A=(CSRdOffTime – CSOnTime + (n – 1)×PageBurstAccessTime)×(TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst write: A=(CSWrOffTime – CSOnTime + (n – 1)×PageBurstAccessTime)×(TimeParaGranularity + 1) × GPMC_FCLK 39/
With n being the page burst access number.
27/ B = ClkActivationTime × GPMC_FCLK 39/
28/ For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst read: C = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst write: C = (WrCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
With n being the page burst access number.
29/ For single read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst write: D = (WrCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/

30/ For single read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For burst write: E = (CSWrOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/

31/ For csn falling edge (CS activated):
– Case GpmcFCLKDivider = 0:
  – F = 0.5 × CSExtraDelay × GPMC_FCLK 39/
– Case GpmcFCLKDivider = 1:
  – F = 0.5 × CSExtraDelay × GPMC_FCLK 39/ if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  – F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – F = 0.5 × CSExtraDelay × GPMC_FCLK 39/ if ((CSOnTime – ClkActivationTime) is a multiple of 3)
  – F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK 39/ if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
  – F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK 39/if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

32/ For ADV falling edge (ADV activated):
– Case GpmcFCLKDivider = 0:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/
– Case GpmcFCLKDivider = 1:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/ if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  – G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39 if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
  – G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
  – G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
– Case GpmcFCLKDivider = 0:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/
– Case GpmcFCLKDivider = 1:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/ if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  – G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/ if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
  – G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
  – G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
– Case GpmcFCLKDivider = 0:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/
– Case GpmcFCLKDivider = 1:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/ if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  – G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – G = 0.5 × ADVExtraDelay × GPMC_FCLK 39/ if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
  – G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
  – G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK 39/ if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

TABLE I. Electrical performance characteristics - Continued.

33/ For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):
– Case GpmcFCLKDivider = 0:
  – H = 0.5 × OEExtraDelay × GPMC_FCLK 39/
– Case GpmcFCLKDivider = 1:
  – H = 0.5 × OEExtraDelay × GPMC_FCLK 39/ if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  – H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – H = 0.5 × OEExtraDelay × GPMC_FCLK 39/ if ((OEOnTime – ClkActivationTime) is a multiple of 3)
  – H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK 39/ if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
  – H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK 39/ if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

For OE rising edge (OE deactivated):
– Case GpmcFCLKDivider = 0:
  – H = 0.5 × OEExtraDelay × GPMC_FCLK 39/
– Case GpmcFCLKDivider = 1:
  – H = 0.5 × OEExtraDelay × GPMC_FCLK 39/if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  – H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – H = 0.5 × OEExtraDelay × GPMC_FCLK 39/ if ((OEOffTime – ClkActivationTime) is a multiple of 3)
  – H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK 39/ if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
  – H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK 39/ if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

34/ For WE falling edge (WE activated):
– Case GpmcFCLKDivider = 0:
  – I = 0.5 × WEExtraDelay × GPMC_FCLK 39/
– Case GpmcFCLKDivider = 1:
  – I = 0.5 × WEExtraDelay × GPMC_FCLK 39/ if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  – I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – I = 0.5 × WEExtraDelay × GPMC_FCLK 39/ if ((WEOnTime – ClkActivationTime) is a multiple of 3)
  – I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK 39/ if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
  – I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK 39/ if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)

For WE rising edge (WE deactivated):
  – Case GpmcFCLKDivider = 0:
  – I = 0.5 × WEExtraDelay × GPMC_FCLK 39/
  – Case GpmcFCLKDivider = 1:
  – I = 0.5 × WEExtraDelay × GPMC_FCLK 39/ if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  – I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK 39/ otherwise
– Case GpmcFCLKDivider = 2:
  – I = 0.5 × WEExtraDelay × GPMC_FCLK 39/ if ((WEOffTime – ClkActivationTime) is a multiple of 3)
  – I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK 39/ if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
  – I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK 39/ if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

35/ J = GPMC_FCLK 39/
36/ In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
37/ P = gpmc_clk period in ns.
38/ For read: K = (ADVRdOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
For write: K = (ADVWrOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK 39/
39/ GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
40/ Related to the gpmc_clk output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.
41/ The jitter probability density can be approximated by a Gaussian function.

TABLE I. Electrical performance characteristics - Continued.

42/ The internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.
43/ Internal parameters are referred to the GPMC functional internal clock which is not provided externally.
44/ GPMC_FCLK is general-purpose memory controller internal functional clock.
45/ The FA5 parameter shows the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
46/ The FA20 parameter shows amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
47/ The FA21 parameter shows amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
48/ P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK 50/
49/ H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK 50/
50/ GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
51/ For single read: A = (CSRdOffTime – CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK 50/
For single write: A = (CSWrOffTime – CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK 50/
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 50/
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 50/ with n being the page burst access number
52/ For reading: B = ((ADVRdOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
For writing: B = ((ADVWrOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPC_FCLK 50/
53/ C = ((OEOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
54/ D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK 50/
55/ E = ((WEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
56/ F = ((WEOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
57/ G = Cycle2CycleDelay × GPMC_FCLK 50/
58/ I = ((OEOffTime + (n – 1) × PageBurstAccessTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
59/ J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK 50/
60/ K = ((ADVOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
61/ L = ((OEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
62/ For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK 50/
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK 50/
For burst read: N = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 50/
For burst write: N = (WrCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK 50/
63/ In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
64/ Internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.
65/ Internal parameters are referred to the GPMC functional internal clock which is not provided externally.
66/ The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
67/ J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK 50/
68/ A = (WEOffTime – WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK 50/
69/ B = ((WEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
70/ C = ((WEOnTime – ADVOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – ADVExtraDelay)) × GPMC_FCLK 50/
71/ D = (WEOnTime × (TimeParaGranularity + 1) + 0.5 × WEExtraDelay) × GPMC_FCLK 50/
72/ E = ((WrCycleTime – WEOffTime) × (TimeParaGranularity + 1) – 0.5 × WEExtraDelay) × GPMC_FCLK 50/

TABLE I. Electrical performance characteristics - Continued.

73/ F = ((ADVWrOffTime – WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – WEExtraDelay)) × GPMC_FCLK 50/
74/ G = ((CSWrOffTime – WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay – WEExtraDelay)) × GPMC_FCLK 50/
75/ H = WrCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK 50/
76/ I = ((OEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK 50/
77/ K = (OEOffTime – OEOnTime) × (1 + TimeParaGranularity) × GPMC_FCLK 50/
78/ L = RdCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK 50/
79/ M = ((CSRdOffTime – OEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay – OEExtraDelay)) × GPMC_FCLK 50/
80/ In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
81/ If the LPDDR interface is operated with a clock frequency less than 200 MHz, lower-speed grade LPDDR devices may be used if the minimum clock period specified for the LPDDR device is less than or equal to the minimum clock period selected for the AM3358-EP LPDDR interface.
82/ For the LPDDR device BGA pad size, see the LPDDR device manufacturer documentation.
83/ A 20-10 via may be used if enough power routing resources are available. An 18-10 via allows for more flexible power routing to the AM3358-EP device.
84/ Zo is the nominal singled-ended impedance selected for the PCB.
85/ This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Zo defined by the single-ended impedance parameter.
86/ Tighter impedance control is required to ensure flight time skew is minimal.
87/ LPDDR keepout region to encompass entire LPDDR routing area.
88/ For dimension definitions, see Figure 49.
89/ Measurements from center of AM3358-EP device to center of LPDDR device.
90/ For single-memory systems, TI recommends that Y offset be as small as possible.
91/ w is defined as the signal trace width.
92/ Non-LPDDR signals allowed within LPDDR keepout region provided they are separated from LPDDR routing layers by a ground plane.
93/ These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors
94/ Only used when two LPDDR devices are used.
95/ LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.
96/ An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
97/ These devices should be placed as close as possible to the device being bypassed.
98/ Per LPDDR device.
99/ Only series termination is permitted.
100/ Zo is the LPDDR PCB trace characteristic impedance.
101/ Series termination values larger than typical only recommended to address EMI issues.
102/ Series termination values should be uniform across net class.
103/ CK represents the clock net class, and ADDR_CTRL represents the address and control signal net class.
104/ Series terminator, if used, should be located closest to the AM3358-EP device.
105/ Differential impedance should be Zo x 2, where Zo is the single-ended impedance defined in Table 1 “PCB Stackup Specifications” sheet 33.
106/ Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion
107/ CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.
108/ DQS[x] represents the DQS0 and DQS1 clock net classes, and DQ[x] represents the DQ0 and DQ1 signal net classes.
109/ Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
110/ There is no requirement for skew matching between data bytes; that is, from net classes DQS0 and DQ0 to net classes DQS1 and DQ1.
111/ Signals from one DQ net class should be considered other LPDDR traces to another DQ net class.
112/ DQLM is the longest Manhattan distance of each of the DQS[x] and DQ[x] net classes.

TABLE I. Electrical performance characteristics - Continued.

113/ The JEDEC JESD79-2F specification defines the maximum clock period of 8 ns for all standard-speed bin DDR2 memory devices. Therefore, all standard-speed bin DDR2 memory devices are required to operate at 125 MHz.
114/ If the DDR2 interface is operated with a clock frequency less than 266 MHz, lower-speed grade DDR2 devices may be used if the minimum clock period specified for the DDR2 device is less than or equal to the minimum clock period selected for the AM3358-EP DDR2 interface.
115/ Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
116/ 92-terminal devices are also supported for legacy reasons. New designs will migrate to 84-terminal DDR2 devices. Electrically, the 92- and 84-terminal DDR2 devices are the same.
117/ For the DDR2 device BGA pad size, see the DDR2 device manufacturer documentation.
118/ A 20-10 via may be used if enough power routing resources are available. An 18-10 via allows for more flexible power routing to the AM3358-EP device.
119/ Zo is the nominal singled-ended impedance selected for the PCB.
120/ This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Zo defined by the single-ended impedance parameter.
121/ Tighter impedance control is required to ensure flight time skew is minimal.
122/ DDR2 keepout region to encompass entire DDR2 routing area.
123/ For dimension definitions, see Figure 53.
124/ Measurements from center of AM3358-EP device to center of DDR2 device.
125/ For single-memory systems, it is recommended that Y offset be as small as possible.
126/ w is defined as the signal trace width.
127/ Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.
128/ These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed(HS) bypass capacitors.
129/ Only used when two DDR2 devices are used.
130/ LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.
131/ An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
132/ These devices should be placed as close as possible to the device being bypassed.
133/ Per DDR2 device.
134/ Only series termination is permitted.
135/ Series termination values larger than typical only recommended to address EMI issues.
136/ Series termination values should be uniform across net class.
137/ Zo is the DDR2 PCB trace characteristic impedance.
138/ No external termination resistors are allowed and ODT must be used for these net classes.
139/ CK represents the clock net class, and ADDR_CTRL represents the address and control signal net class.
140/ Series terminator, if used, should be located closest to the AM3358-EP device.
141/ Differential impedance should be Zo x 2, where Zo is the single-ended impedance defined in table" PCB Stackup Specifications" sheet 36 herein .
142/ Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
143/ CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.
144/ DQS[x] represents the DQS0 and DQS1 clock net classes, and DQ[x] represents the DQ0 and DQ1 signal net classes.
145/ There is no requirement for skew matching between data bytes; that is, from net classes DQS0 and DQ0 to net classes DQS1 and DQ1.
146/ Signals from one DQ net class should be considered other DDR2 traces to another DQ net class.
147/ DQLM is the longest Manhattan distance of each of the DQS[x] and DQ[x] net classes.
148/ The JEDEC JESD209B specification only defines the maximum clock period for LPDDR333 and faster speed bin LPDDR memory devices. To determine the maximum clock period, see the respective LPDDR memory data sheet.
149/ The JEDEC JESD79-3F Standard defines the maximum clock period of 3.3 ns for all standard-speed bin DDR3 and DDR3L memory devices. Therefore, all standard-speed bin DDR3 and DDR3L memory devices are required to operate at 303 MHz.

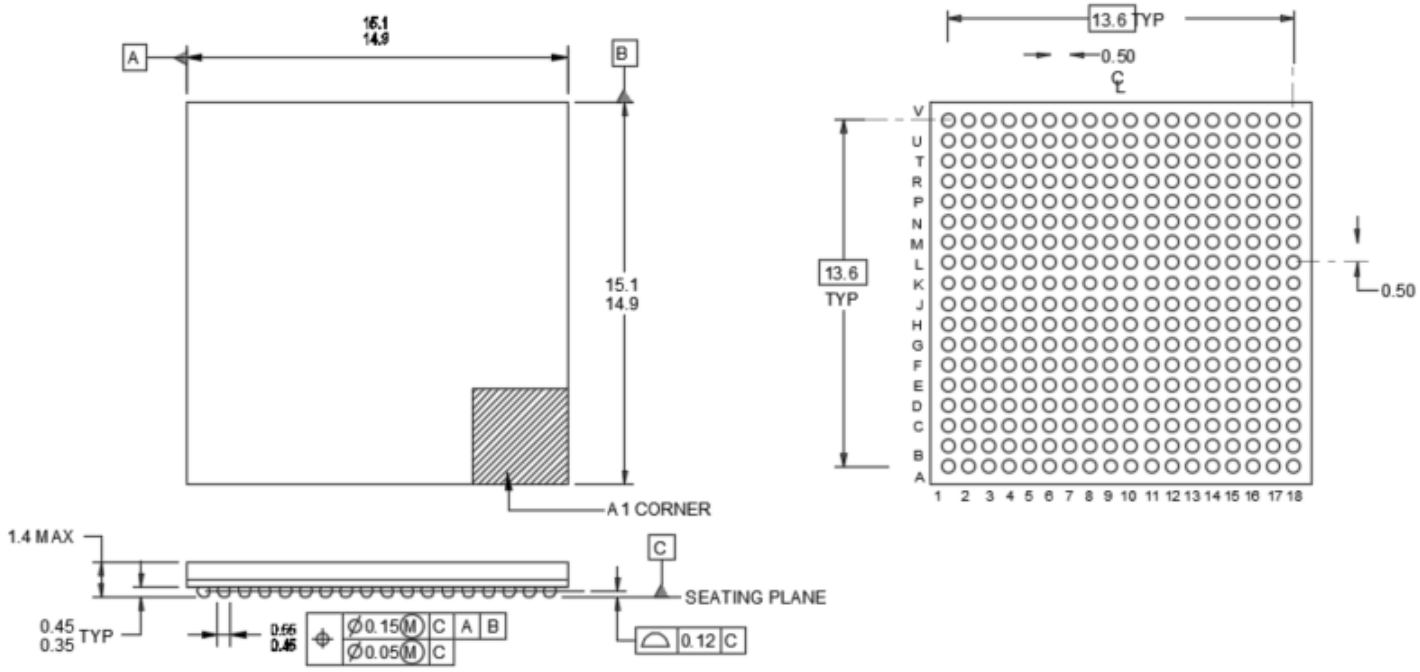
TABLE I. Electrical performance characteristics - Continued.

150/ For valid DDR3 device configurations and device counts, see manufacturer data Section 7.7.2.3.3.1, Figure 7-47 and Figures 7-49.
151/ For the DDR3 device BGA pad size, see the DDR3 device manufacturer documentation.
152/ Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.
153/ No traces should cross reference plane cuts within the DDR3 routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.
154/ Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.
155/ An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.
156/ Zo is the nominal singled-ended impedance selected for the PCB.
157/ This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Zo defined by the single-ended impedance parameter.
158/ Tighter impedance control is required to ensure flight time skew is minimal.
159/ DDR3 keepout region to encompass entire DDR3 routing area.
160/ For dimension definitions, see manufacturer data Figure 7-50.
161/ Measurements from center of AM3358-EP device to center of DDR3 device.
162/ Minimizing X1 and Y improves timing margins.
163/ w is defined as the signal trace width.
164/ Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.
165/ These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high speed (HS) bypass capacitors and DDR3 signal routing.
166/ Only used when two DDR3 devices are used.
167/ LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.
168/ Closer and shorter is better.
169/ Measured from the nearest AM3358-EP VDDS_DDR and ground terminal to the center of the capacitor package.
170/ Three of these capacitors should be located underneath the AM3358-EP device, between the cluster of VDDS_DDR and ground terminals, between the DDR3 interfaces on the package.
171/ Measured from the DDR3 device power and ground terminal to the center of the capacitor package.
172/ Per DDR3 device.
173/ An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.
174/ An HS bypass capacitor may share a via with a DDR3 device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR3 device pad should be less than 150 mils.
175/ Up to a total of two pairs of DDR3 power and ground terminals may share a via.
176/ CK represents the clock net class, and ADDR_CTRL represents the address and control signal net class.
177/ The use of vias should be minimized.
178/ Additional bypass capacitors are required when using the VDDS_DDR plane as the reference plane to allow the return current to jump between the VDDS_DDR plane and the ground plane when the net class switches layers at a via.
179/ Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).
180/ Non-mirrored configuration (all DDR3 memories on same side of PCB).
181/ While this length can be increased for convenience, its length should be minimized.
182/ ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.
183/ CK net class only.
184/ CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes + 300 mils. For definition, see manufacturer data Section 7.7.2.3.6.1 and Figure 58 herein.
185/ Center-to-center spacing is allowed to fall to minimum (w) for up to 1250 mils of routed length.
186/ Signals from one DQ net class should be considered other DDR3 traces to another DQ net class.
187/ CK spacing set to ensure proper differential impedance. Differential impedance should be Zo x 2, where Zo is the single-ended impedance defined in manufacturer data in Table 7-60.
188/ Source termination (series resistor at driver) is specifically not allowed.
189/ Termination values should be uniform across the net class.

TABLE I. Electrical performance characteristics - Continued.

190/ DQS[x] represents the DQS0 and DQS1 clock net classes, and DQ[x] represents the DQ0 and DQ1 signal net classes.
191/ External termination disallowed. Data termination should use built-in ODT functionality
192/ DQLMn is the longest Manhattan distance of a byte. For definition, see manufacturer data on Section 7.7.2.3.6.2 and Figure 59
193/ DQLM0 is the longest Manhattan length for the DQ0 net class.
194/ DQLM1 is the longest Manhattan length for the DQ1 net class.
195/ Length matching is only done within a byte. Length matching across bytes is not required.
196/ Each DQS clock net class is length matched to its associated DQ signal net class.
197/ Center-to-center spacing is allowed to fall to minimum for up to 1250 mils of routed length.
198/ Other DDR3 trace spacing means signals that are not part of the same DQ[x] signal net class.
199/ This applies to spacing within same DQ[x] signal net class.
200/ DQS[x] pair spacing is set to ensure proper differential impedance. Differential impedance should be Zo x 2, where Zo is the singleended impedance defined in manufacturer data in Table 7-60
201/ A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device stretches the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max} + t_{su(SDA-SCLH)} = 1000 + 250 = 1250$ ns (according to the standard-mode I^2C-Bus Specification) before the SCL line is released.
202/ A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
203/ The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal
204/ Except when specified otherwise.
205/ ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
206/ P = McASP[x]_AHCLKR and McASP[x]_AHCLKX period in nanoseconds (ns).
207/ R = McASP[x]_ACLKR and McASP[x]_ACLKX period in ns.
208/ P = SPI_CLK period.
209/ This timing applies to all configurations regardless of MCSPIX_CLK polarity and which clock edges are used to drive output data and capture input data.
210/ Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.
211/ Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.
212/ The polarity of SPIx_CLK and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable:
– SPIx_CLK(1) phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 1 (Modes 1 and 3).
– SPIx_CLK(1) phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 0 (Modes 0 and 2).
213/ Case P = 20.8 ns, A = (TCS + 1) × TSPICLKREF (TCS is a bit field of MCSPI_CH(i)CONF register).
Case P > 20.8 ns, A = (TCS + 0.5) × Fratio × TSPICLKREF (TCS is a bit field of MCSPI_CH(i)CONF register).
Note: P = SPI_CLK clock period.
214/ B = (TCS + 0.5) × TSPICLKREF × Fratio (TCS is a bit field of MCSPI_CH(i)CONF register, Fratio: Even ≥ 2).
215/ P = MMC_CLK period.
216/ P = L3_CLK (PRU-ICSS ocp clock) period.
217/ n = 16
218/ n = 15
219/ Except when specified otherwise.
220/ U = UART baud time = 1/programmed baud rate.

Case X



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.
2. This drawing is subject to change without notice.
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see manufacturer data number SPRAA99.
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

FIGURE 1. Case outline.

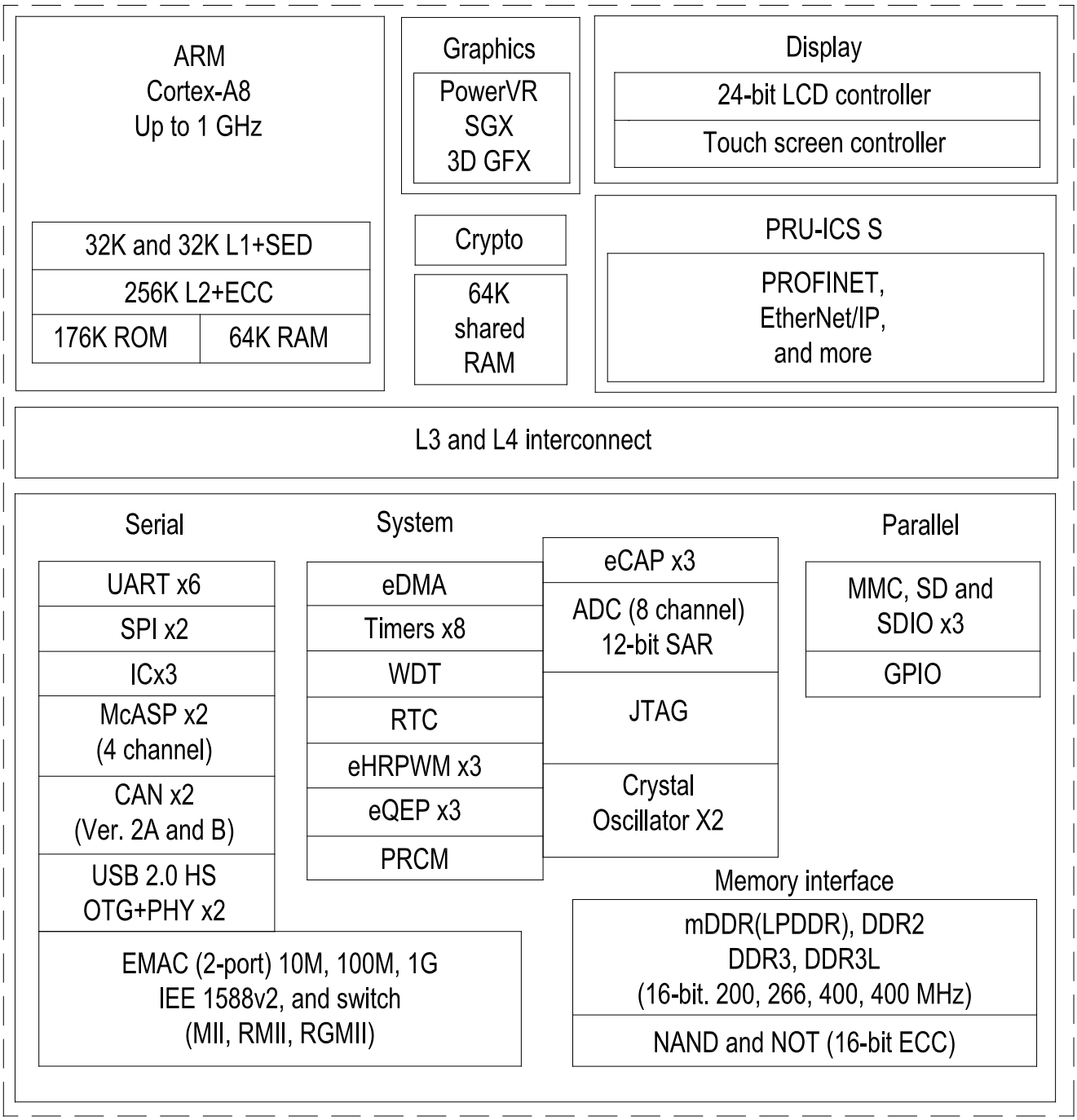


FIGURE 2. Functional block diagram.

	A	B	C	D	E	F
18	VSS	EXTINTe	EXAP0_IN_PWMC_OUT	UARTI_CTSn	UART0_CTSn	MMC0_DAT2
17	SPI0_SCLK	SPI0_D0	I2C0_SDA	UART1_RTSn	UART0_RTSn	MMC0_DAT3
16	SPI0_CSD	SPI0_D1	I2C0_SCL	UART1_RXD	UART0_TXD	USB0_DRVVBUS
15	ZDMA_EVENT_INTR0	PWRONRSTn	SPI0_CS1	UART1_TXD	UART0_RXD	USB1_DRVVBUS
14	MCASP0_AHCLKX	EMU1	EMU0	XDMA_EVENT_INTR1	VDDS	VDDSHV6
13	MCASP0_ACLKX	MCASP0_FSX	MCASP0_FSR	MCASP0_AXR1	VDDSHV6	VDD_MPU
12	TCK	MCASP0_ACLKR	MCASP0_ACLKR	MCASP0_AXR0	VDDSHV6	VDD_MPU
11	TDO	TDI	TMS	CAP_VDD_SRAM_MPU	VDDSHV6	VDD_MPU
10	WARMRSTn	TRSTn	CAP_VBB_MPU	VDDS_SRAM_MPU_BB	VDDSHV6	VDD_MPU
9	VREFN	VREFP	AIN7	CAP_VDD_SRAM_CORE	VDDS_SRAM_CORE_BG	VDDS
8	AIN6	AIN5	AIN4	VDDA_ADC	VSSA_ADC	VSS
7	AIN3	AIN2	AIN1	VDDS_RTC	VDDS_PLL_DRR	VDD_CORE
6	RTC_XTALIN	AIN0	PMIC_POWER_EN	CAP_VDD_RTC	VDDS	VDD_CORE
5	VSS_RTC	RTC_KALDO_ENu	EXT_WAKEUP	DDR_A6	DDR_A2	DDR_A10
4	RTC_XTALOUT	RTC_KALDO_ENu	DDR_BA0	DDR_A8	DDR_A12	DDR_A0
3	RESERVED	DDR_BA2	DDR_A3	DDR_A15	DDR_A12	DDR_A0
2	VDO_MPU_MON	DDR_WEn	DDR_A4	DDR_CK	DDR_A7	DDR_A11
1	VSS	DDR_A5	DDR_A9	DDR_CKn	DDR_BA1	DDR_CASn

FIGURE 3. Pin Map Location (Section Left)

	G	H	J	K	L	M
18	MMC0_CMD	RMII1_REF_CLK	MII1_TXD3	MII1_TX_CLK	MII1_RX_CLK	MDC
17	MMC0_CLK	MII1_CRS	MII1_CRS	MII1_TXD0	MII1_RXD3	MDIO
16	MMC0_DAT0	MII1_COL	MII1_TX_EN	MII1_TXD1	MII1_RXD2	MII1_RXD0
15	MMC0_DAT1	VDDS_PLL_MPU	MII1_RX_ER	MII1_TXD2	MII1_RXD1	USB0_CE
14	VDDSHV6	VDDSHV4	VDDSHV4	VDDSHV5	VDDSHV5	VSSA_USB
13	VDD_MPU	VDD_MPU	VDD_MPU	VDDS	VSS	VDD_CORE
12	VSS	VSS	VDD_CORE	VDD_CORE	VSS	VSS
11	VSS	VDD_CORE	VSS	VSS	VSS	VDD_CORE
10	VDD_CORE	VSS	VSS	VSS	VSS	VSS
9	VSS	VSS	VSS	VSS	VDD_CORE	VSS
8	VSS	VSS	VSS	VDD_CORE	VDD_CORE	VSS
7	VDD_CORE	VSS	VSS	VSS	VDD_CORE	VSS
6	VDD_CORE	VSS	VSS	VDD_CORE	VDD_CORE	VSS
5	VDDS_DDR	VDDS_DDR	VDDS_DDR	VDDS_DDR	VDD_CORE	VPP
4	DDR_RASn	DDR_A14	VDDS_VREF	DDR_D12	DDR_D14	DDR_D1
3	DDR_CKE	DDR_A13	VDDS_VTP	DDR_D11	DDR_D13	DDR_D0
2	DDR_RESETn	DDR_CSn0	DDR_DQM1	DDR_D10	DDR_DQSn1	DDR_DQS0
1	DDR_ODT	DDR_A1	DDR_D8	DDR_D9	DDR_DQS1	DDR_D15

FIGURE 4. Pin Map Location (Section Middle)

	N	P	R	T	U	V
18	USB0_DM	USB1_CE	USB1_DM	USB1_VBUS	GPMC_BEn1	VSS
17	USB0_DP	USB1_ID	USB1_DP	GPMC_WAIT0	GPMC_WPn	GPMC_A11
16	VDDA1P8V_USB0	USB0_ID	VDDA1P8V_USB1	GPMC_A10	GPMC_A9	GPMC_A8
15	VDDA3P3V_USB0	USB0_VBUS	VDDA3P3V_USB1	GPMC_A7	GPMC_A6	GPMC_A5
14	VSSA_USB	VDDS	GPMC_A4	GPMC_A3	GPMC_A2	GPMC_A1
13	VDD_CORE	VDDSHV3	GPMC_A0	GPMC_CSn3	GPMC_AD15	GPMC_AD14
12	VDD_CORE	VDDSHV3	GPMC_AD13	GPMC_AD12	GPMC_AD11	GPMC_CLK
11	VSS	VDDSHV2	VDDS_OSC	GPMC_AD10	XTALOUT	VSS_OSC
10	VSS	VDDSHV2	VDDS_PLL_CORE_LCD	GPMC_AD9	GPMC_AD8	XTALIN
9	VDD_CORE	VDDS	GPMC_AD6	GPMC_AD7	GPMC_CSn1	GPMC_CSn2
8	VDD_CORE	VDDSHV1	GPMC_AD2	GPMC_AD3	GPMC_AD4	GPMC_AD5
7	VSS	VDDSHV1	GPMC_ADVn_ALE	GPMC_OEn_REn	GPMC_AD0	GPMC_AD1
6	VDDS	VDDSHV6	LCD_AC_BIAS_EN	GPMC_BEn0_CLE	GPMC_WEn	GPMC_CSn0
5	VDDSHV6	VDDSHV6	LCD_HSYNC	LCD_DATA15	LCD_VSYNC	LCD_PCLK
4	DDR_D5	DDR_D7	LCD_DATA3	LCD_DATA7	LCD_DATA11	LCD_DATA14
3	DDR_D4	DDR_D6	LCD_DATA2	LCD_DATA6	LCD_DATA10	LCD_DATA13
2	DDR_D3	DDR_DQSn0	LCD_DATA1	LCD_DATA5	LCD_DATA9	LCD_DATA12
1	DDR_D2	DDR_DQS0	LCD_DATA0	LCD_DATA4	LCD_DATA8	VSS

FIGURE 5. Pin Map Location (Section Right)

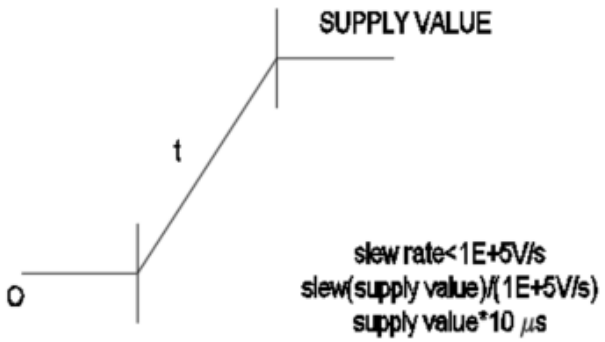
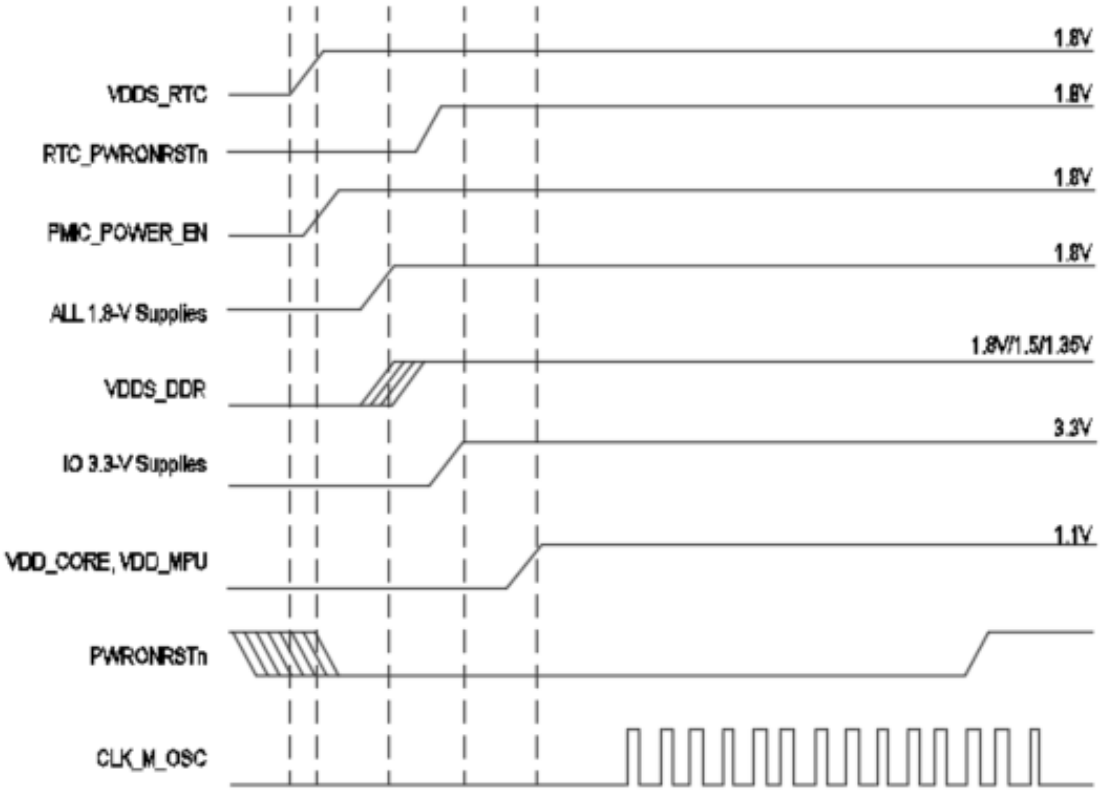


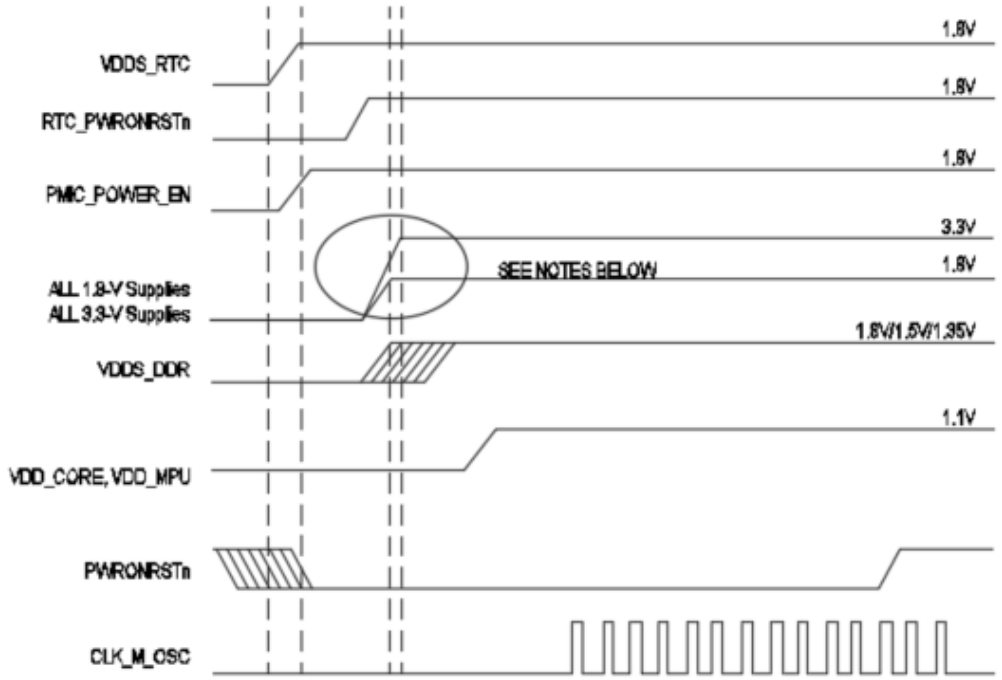
FIGURE 6. Power Supply and Slew Rate.



Notes:

A. RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
B. When using the GCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE.
C. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
D. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V IIO power supplies.
E. VDDS_RTC can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
F. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

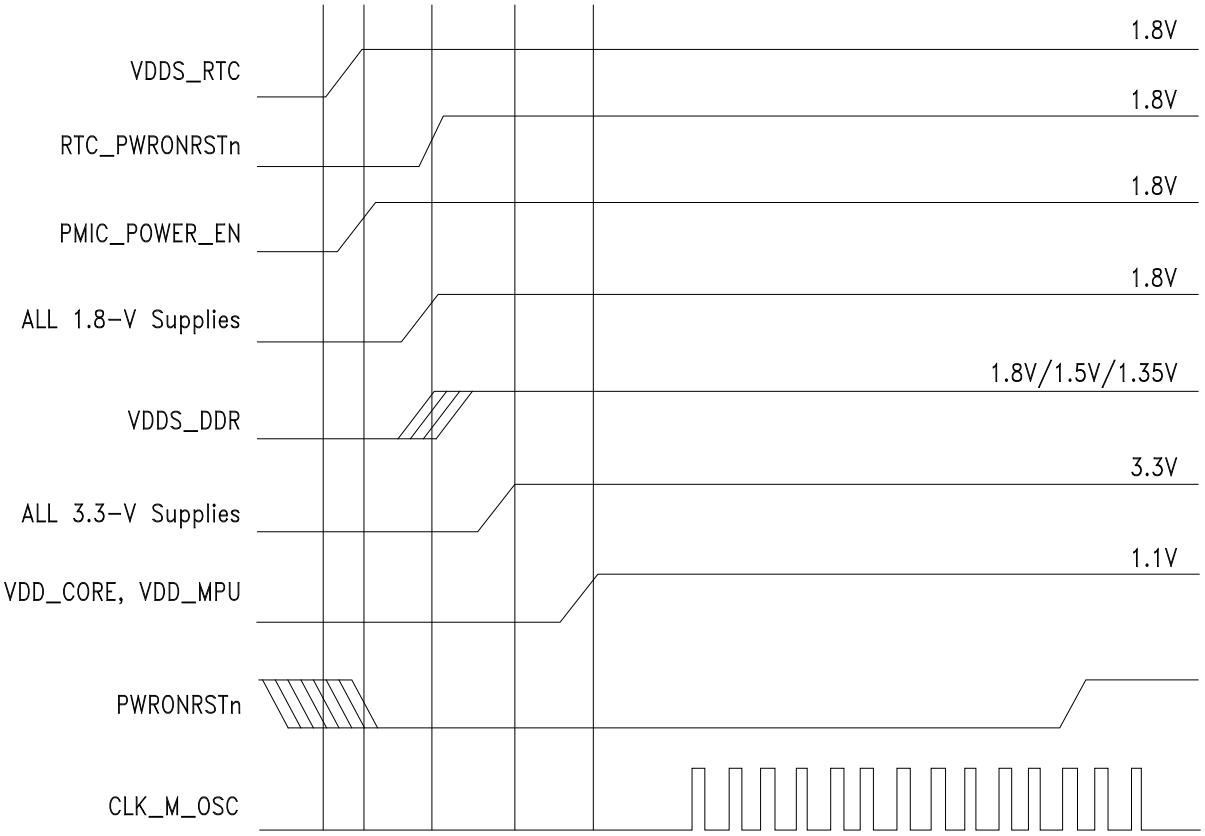
FIGURE 7. Preferred Power Supply Sequencing with Dual Voltage IOs Configured as 3.3 V.



Notes:

A. RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
B. The 3.3-V IO power supplies may be ramped simultaneously with the 1.8-V IO power supplies if the voltage sourced by any 3.3-V power supplies does not exceed the voltage sourced by any 1.8-V power supply by more than 2 V. Serious reliability issues may occur if the system power supply design allows any 3.3-V IO power supplies to exceed any 1.8-V IO power supplies by more than 2 V.
C. When using the GCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE.
D. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
E. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V IO power supplies.
F. VDDS_RTC can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
G. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

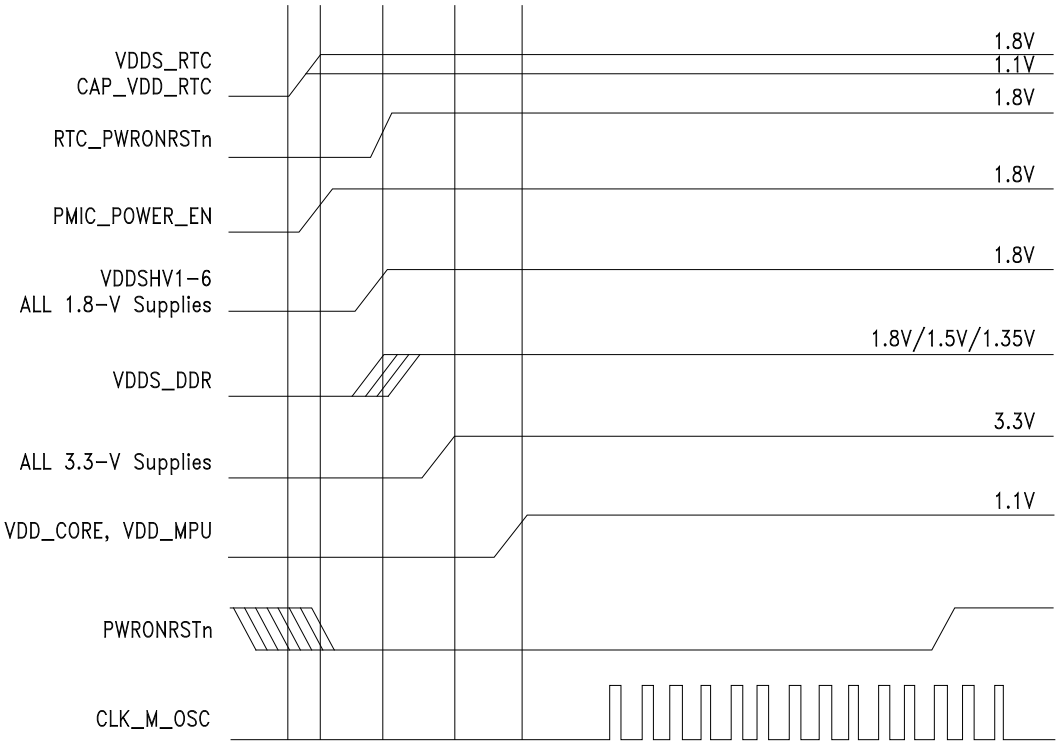
FIGURE 8. Alternate Power-Supply Sequencing with Dual-Voltage IOs Configured as 3.3 V.



Notes:

A. RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
B. When using the GCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE.
C. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
D. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V IO power supplies.
E. VDDS_RTC can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
F. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

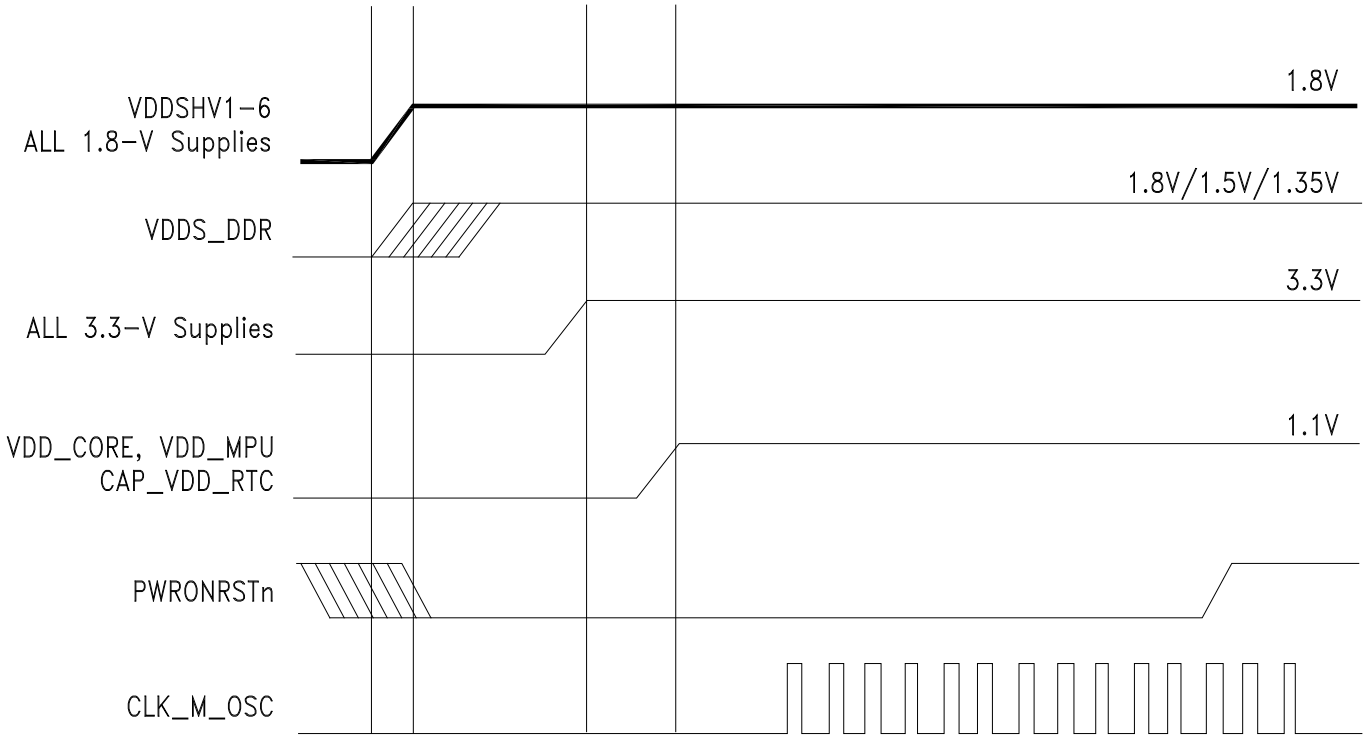
FIGURE 9. Power-Supply Sequencing With Dual-Voltage IOs Configured as 1.8 V.



Notes:

A. RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
B. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC. If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply.
C. When using the GCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE.
D. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
E. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V IO power supplies.
F. VDDS_RTC should be ramped at the same time or before CAP_VDD_RTC, but these power inputs can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
G. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

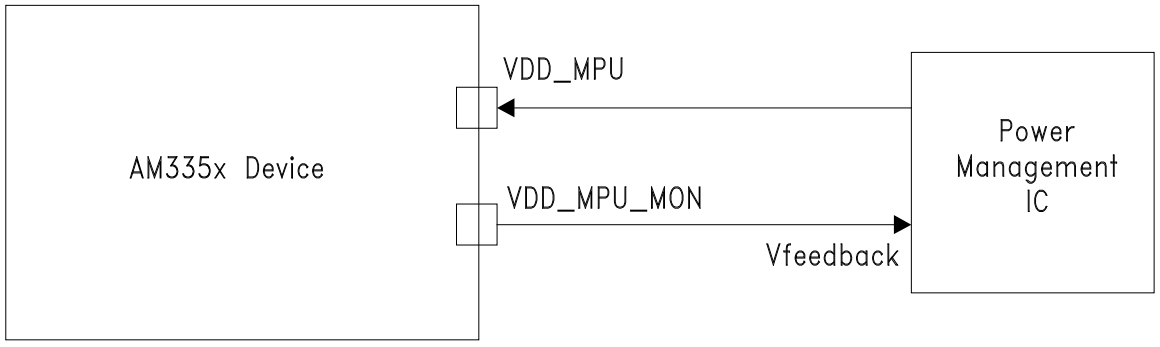
FIGURE 10. Power-Supply Sequencing With Internal RTC LDO Disabled.



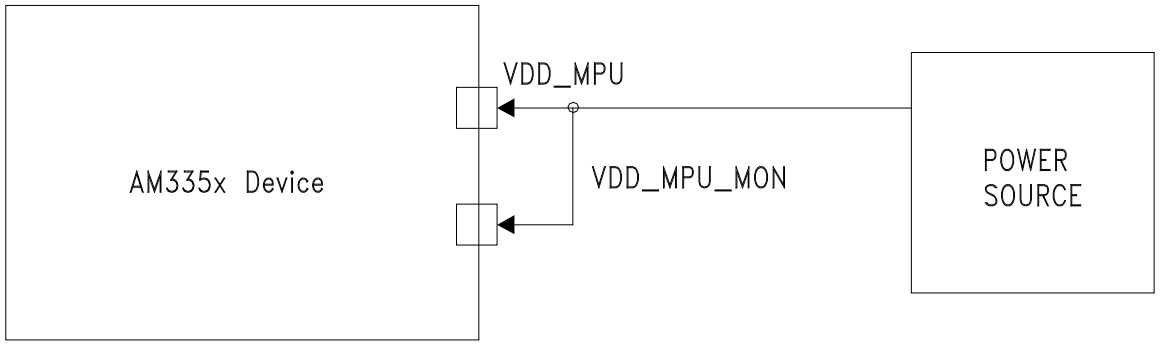
Notes:

A. CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC. If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. The PMIC_POWER_EN output cannot be used when the RTC is disabled.
B. When using the GCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE.
C. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
D. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V IO power supplies.
E. VDDS_RTC should be ramped at the same time or before CAP_VDD_RTC, but these power inputs can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
F. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

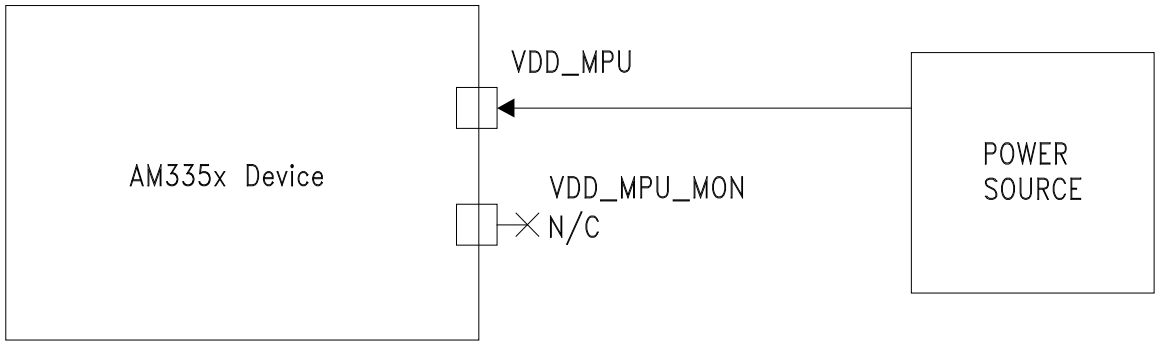
FIGURE 11. Power-Supply Sequencing with RTC Feature Disabled.



Connectioin for VDD_MPU_MON if volrage monitoring is used



Preferred connectioin for VDD_MPU_MON if nolrage monitoring is NOT used



Optional conncection or VDD_MPU_MON if voltage monitoring is NOT used

FIGURE 12. VDD_MPU_MON Connectivity.

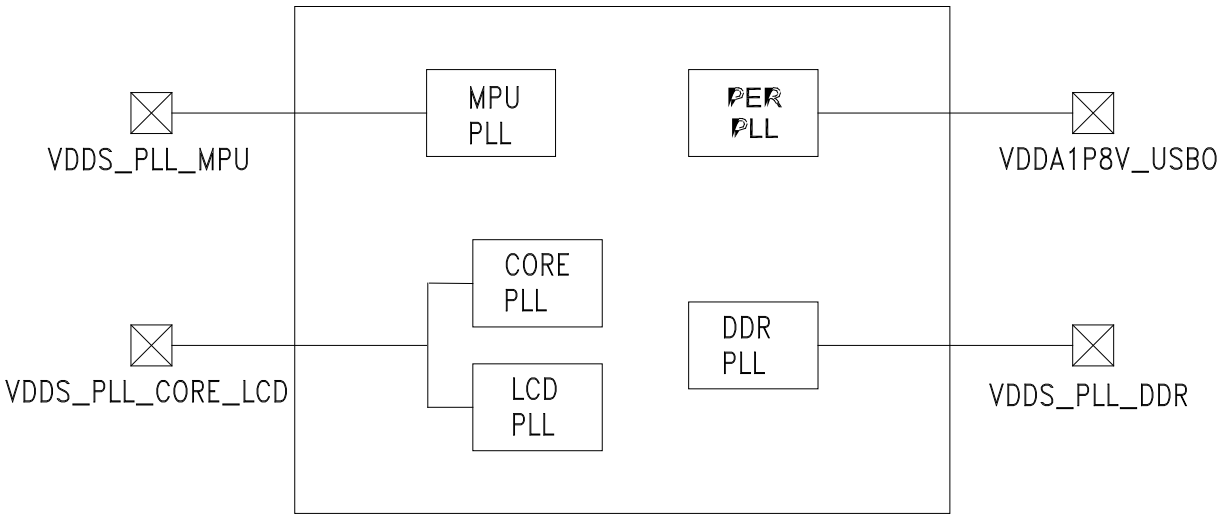


FIGURE 13. DPLL Power Supply Connectivity.

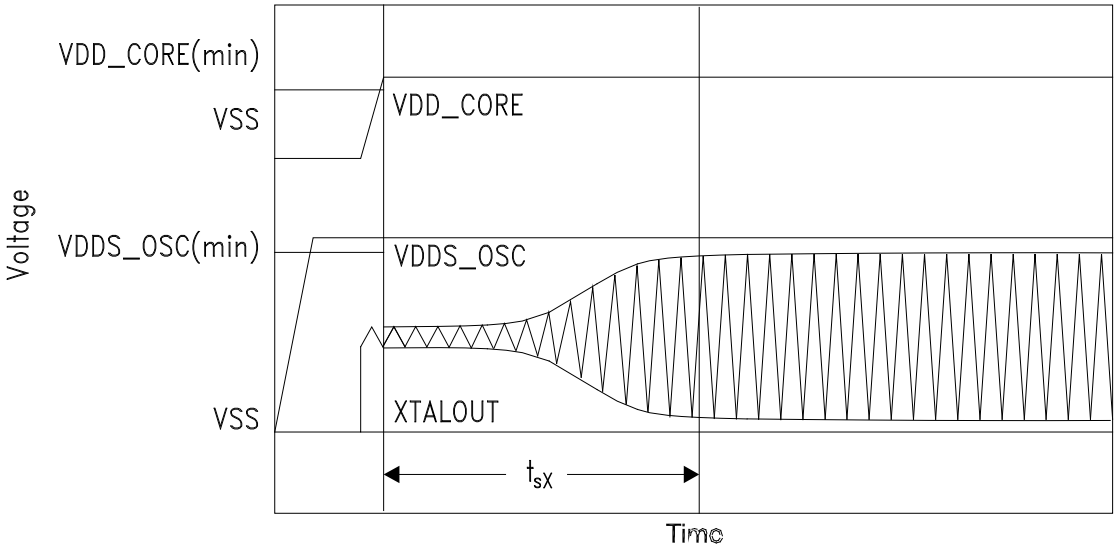


FIGURE 14. OSC0 Start-Up Time.

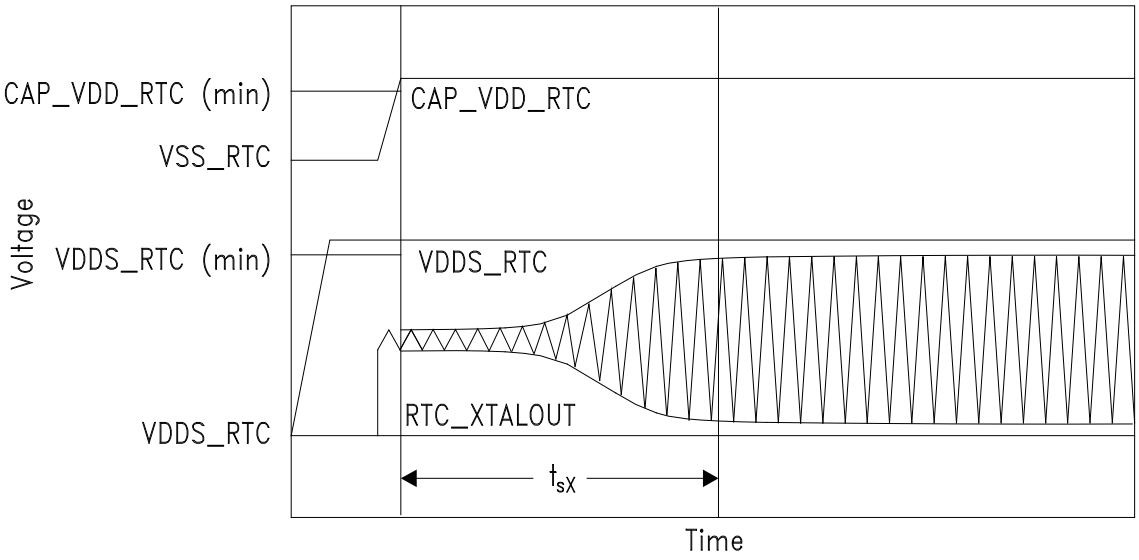


FIGURE 15. OSC1 Start-up Time.

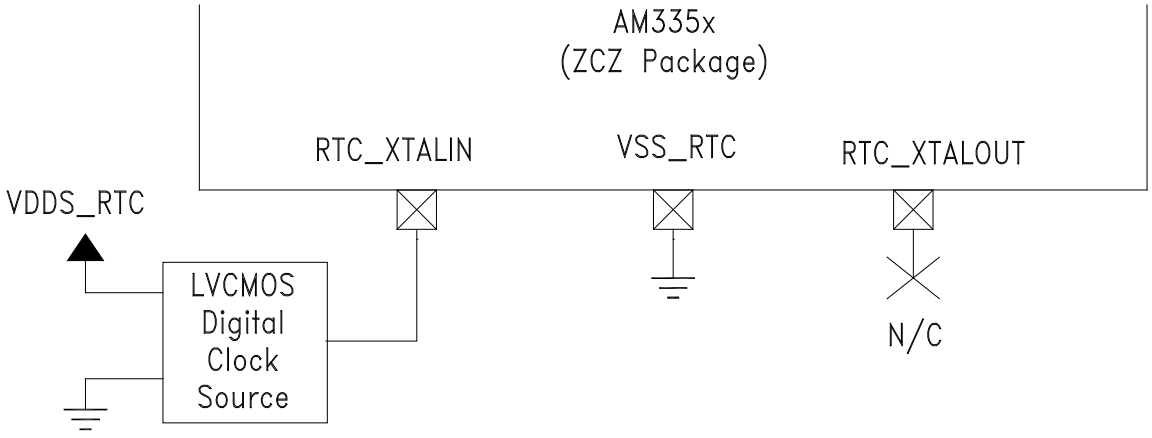


FIGURE 16. OSC1 LVCMOS Circuit Schematic.

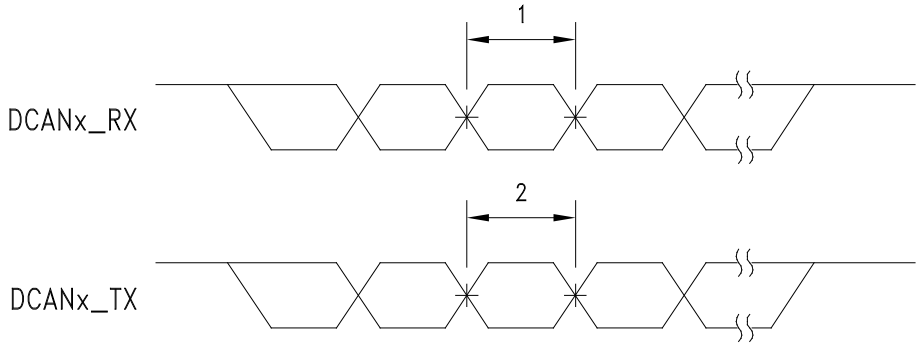


FIGURE 17. DCANx Timings.

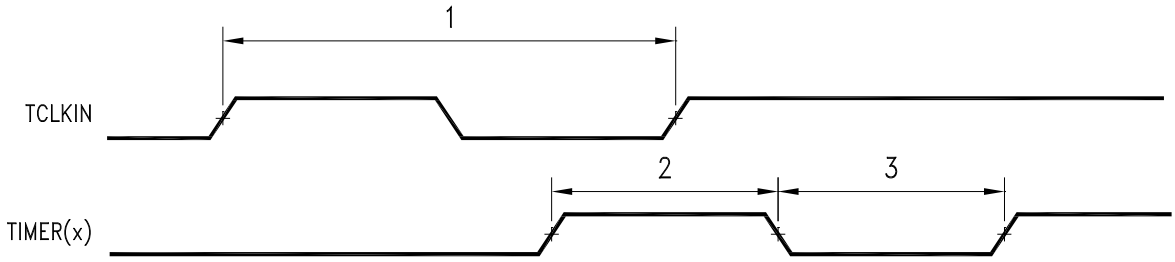


FIGURE 18. Timer Timing.

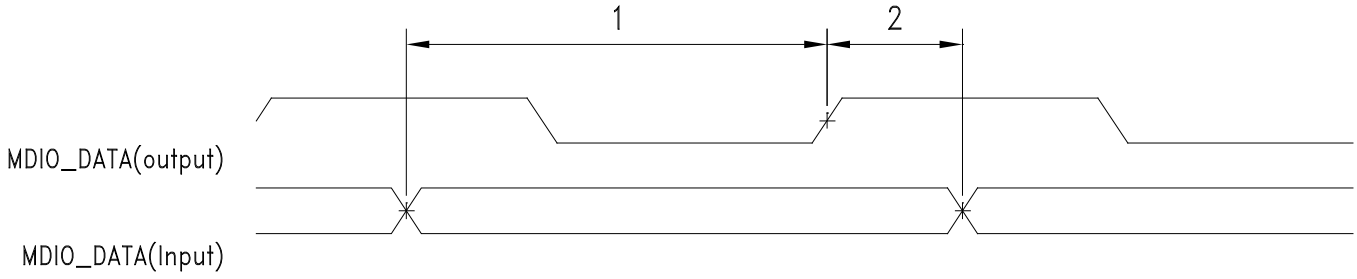


FIGURE 19. MDIO_DATA Timing - Input Mode.

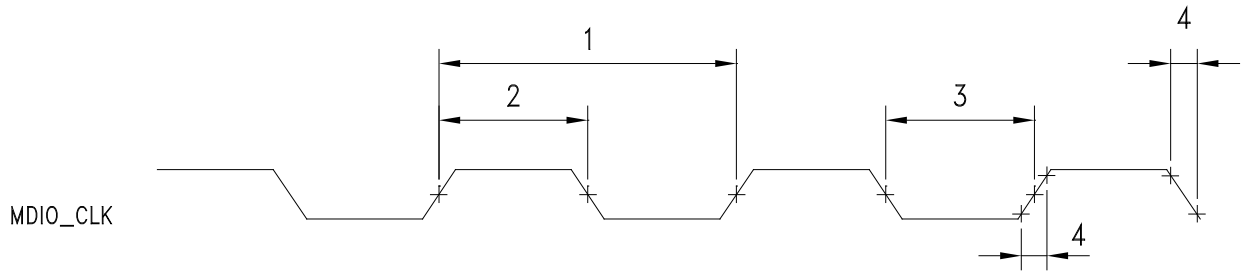


FIGURE 20. MDIO_CLK Timing.

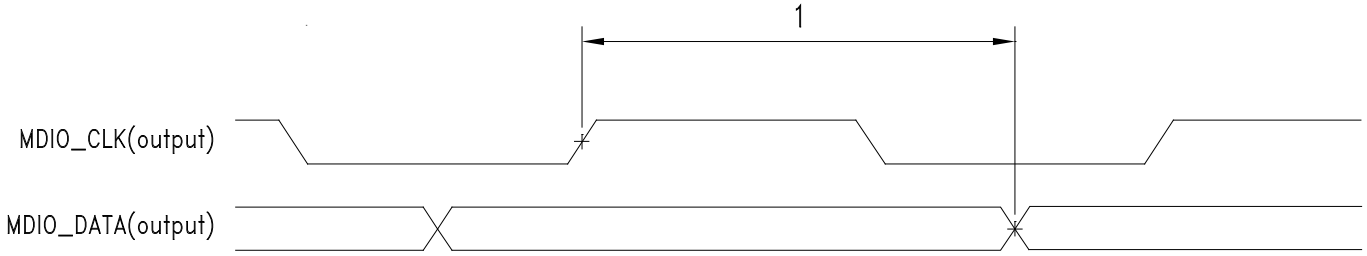


FIGURE 21. MDIO_DATA Timing - Output Mode.

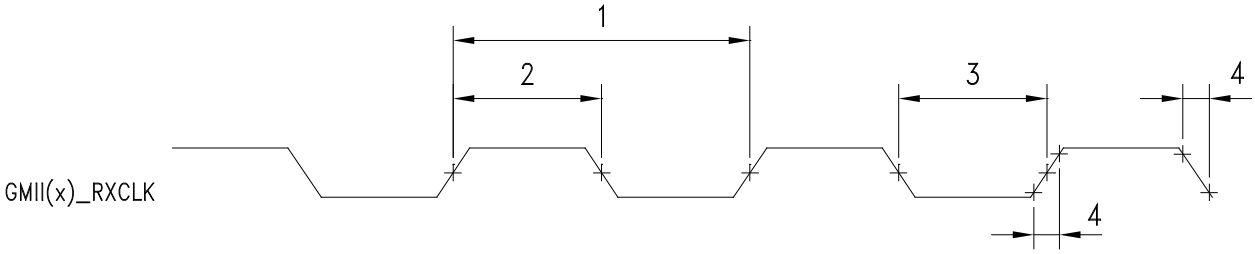


FIGURE 22. GMII[x]_RXCLK Timing - MII Mode.

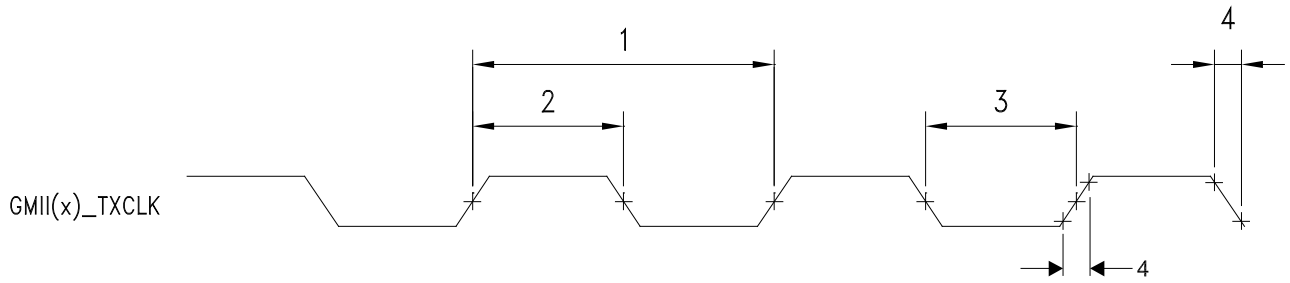


FIGURE 23. GMII[x]_TXCLK Timing - MII Mode.

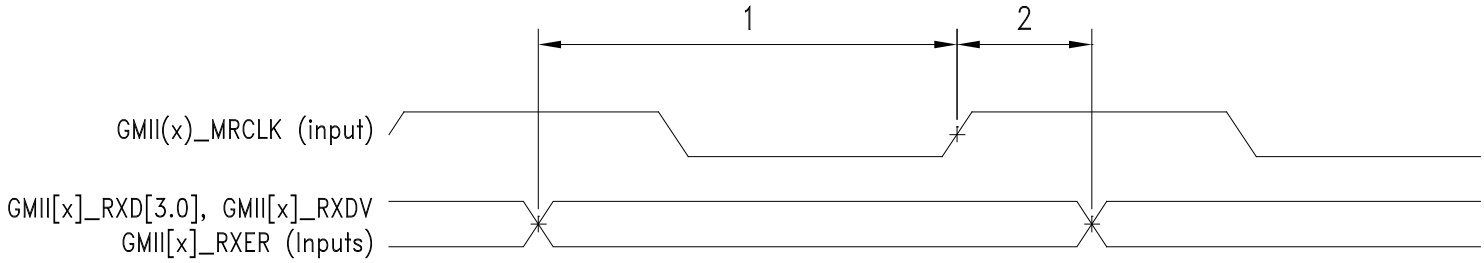


FIGURE 24. GMII[x]_RXD[3:0], GMII[x]_RXDV, GMII[x]_RXER Timing - MII Mode.

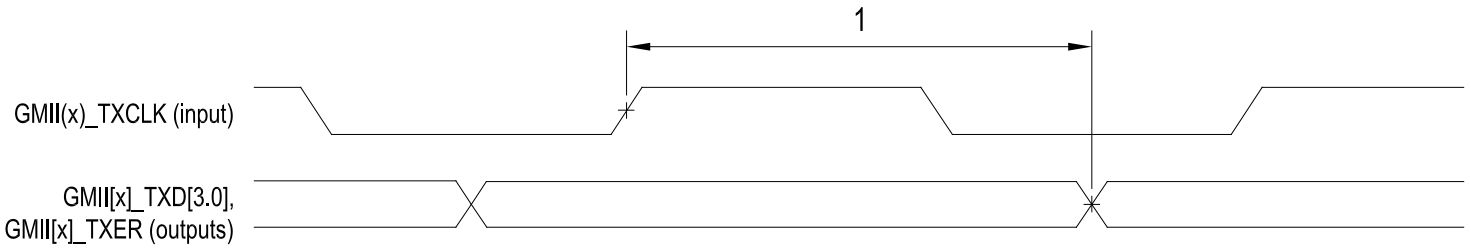


FIGURE 25. GMII[x]_TXD[3:0], GMII[x]_TXEN Timing - MII Mode.

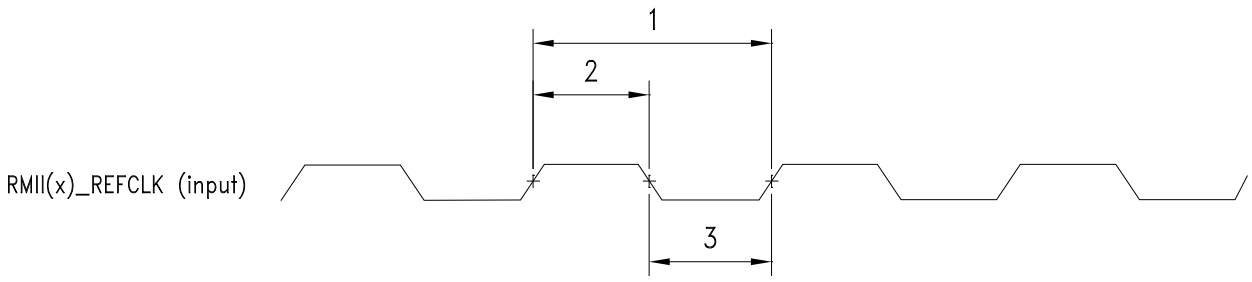


FIGURE 26. RMII[x] REFCLK Timing - RMII Mode.

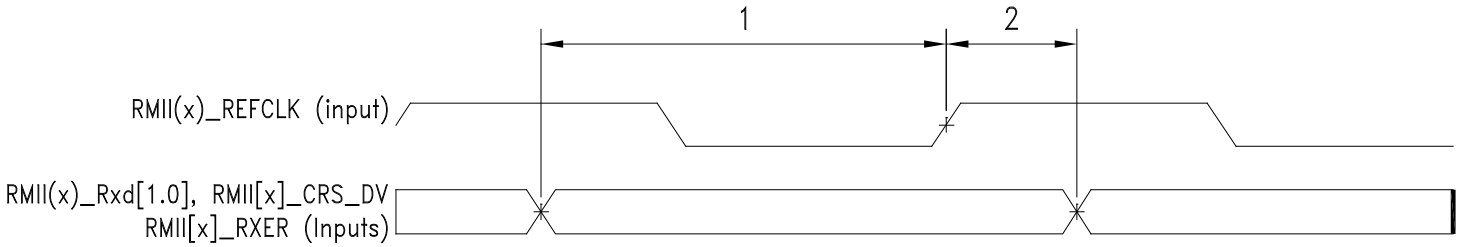


FIGURE 27. RMII[x] RXD[1:0], RMII[x] CRS DV, RMII[x] RXER Timing - RMII Mode.

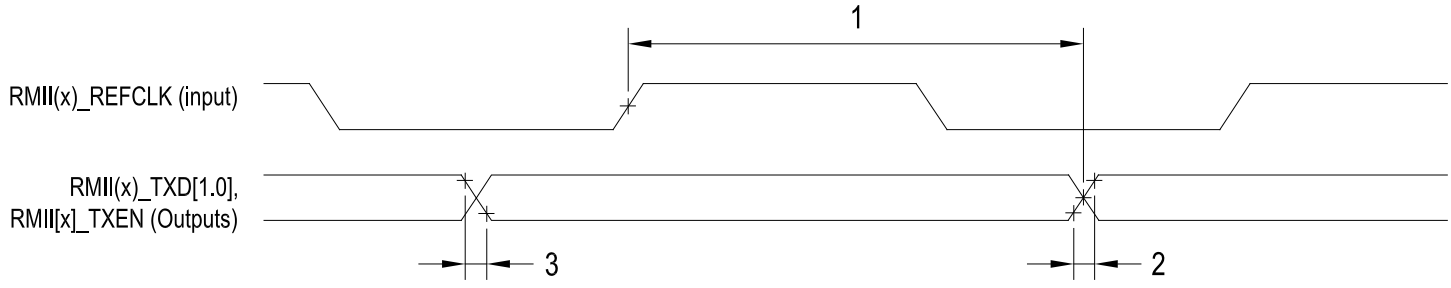


FIGURE 28. RMII[x] TXD[1:0], RMII[x] TXEN Timing - RMII Mode.

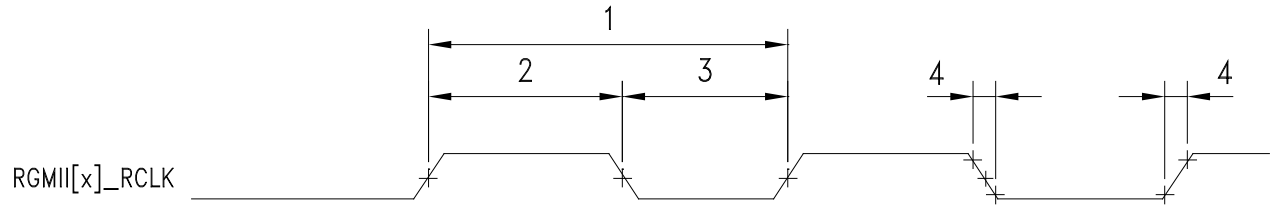
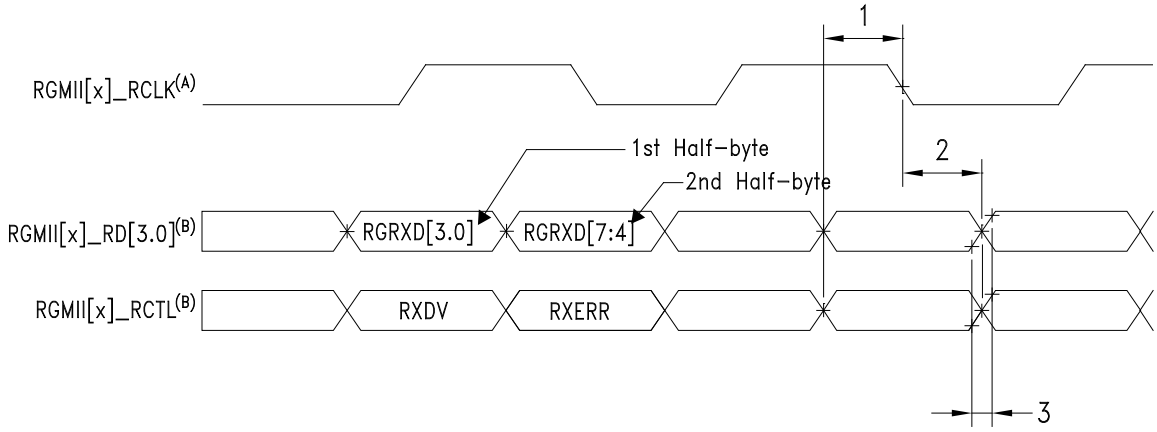


FIGURE 29. RGMII[x] RCLK Timing - RGMII Mode.



Notes:

A. RGMII[x]_RCLK must be externally delayed relative to the RGMII[x]_RD[3:0] and RGMII[x]_RCTL signals to meet the respective timing requirements.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RCLK and data bits 7-4 on the falling edge of RGMII[x]_RCLK. Similarly, RGMII[x]_RCTL carries RXDV on rising edge of RGMII[x]_RCLK and RXERR on falling edge of RGMII[x]_RCLK.

FIGURE 30. RGMII[x]_RD[3:0], RGMII[x]_RCTL Timing - RGMII Mode.

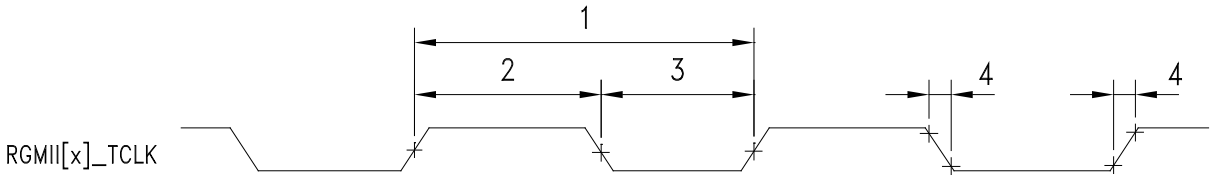
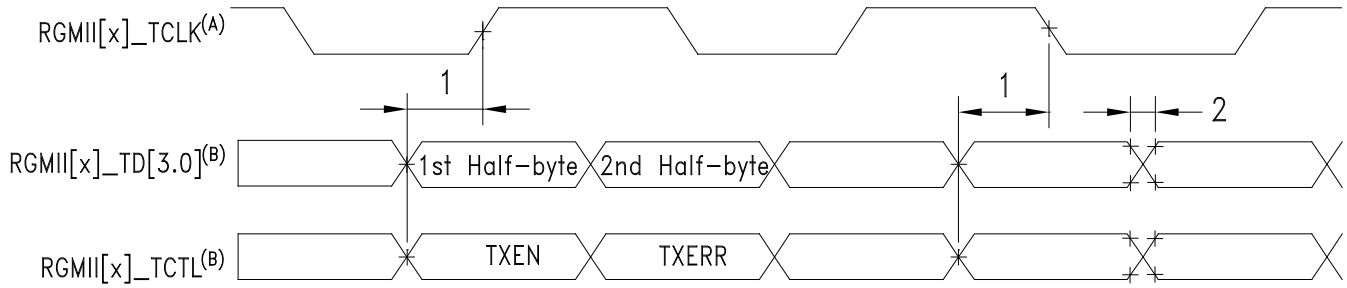


FIGURE 31. RGMII[x]_TCLK Timing - RGMII Mode.

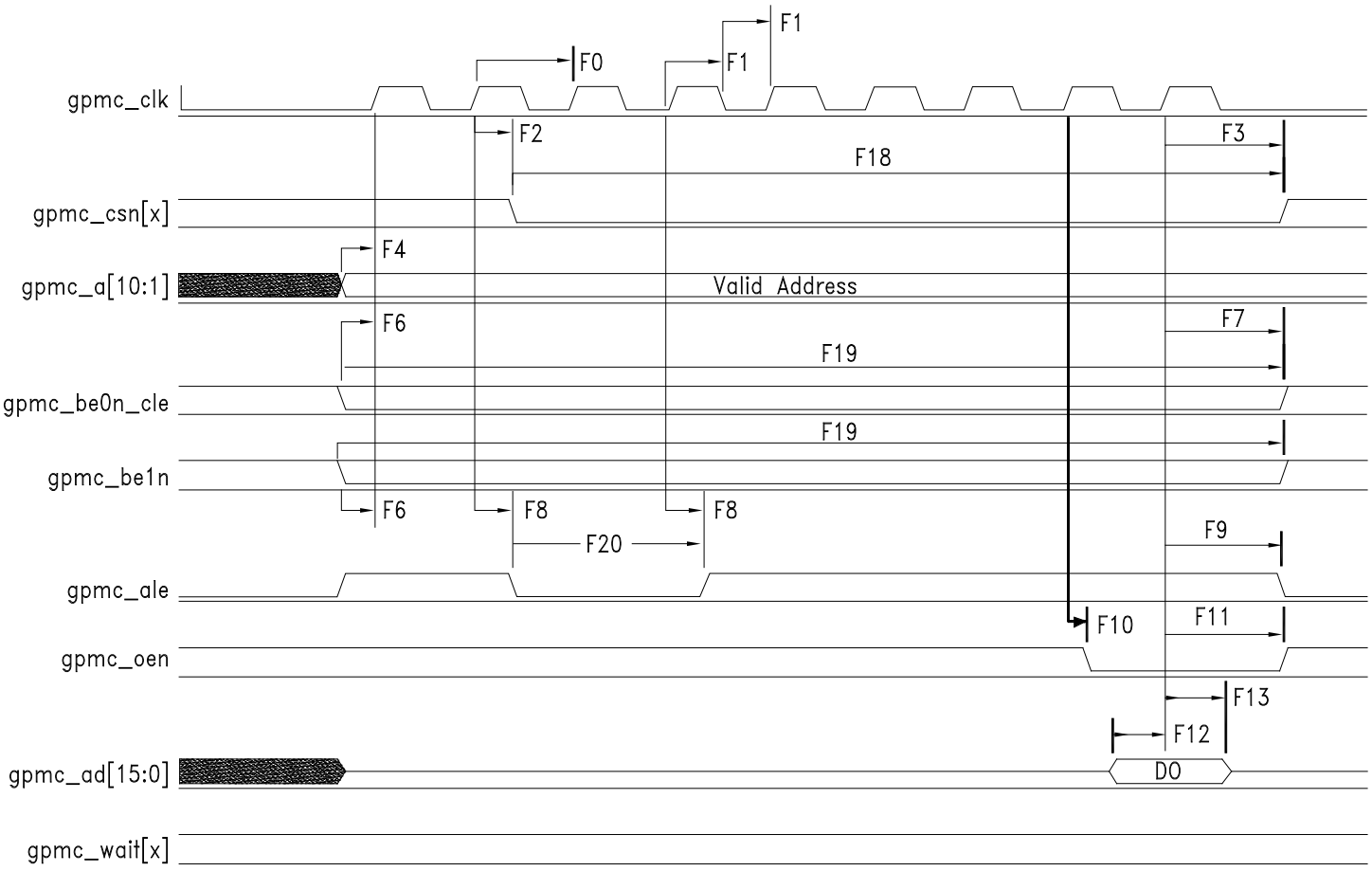


Notes:

A The EMAC and switch implemented in the AM3358-EP device supports internal delay mode, but timing closure was not performed for this mode of operation. Therefore, the AM3358-EP device does not support internal delay mode.

B. Data and control information is transmitted using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TCLK and data bits 7-4 on the falling edge of RGMII[x]_TCLK. Similarly, RGMII[x]_TCTL carries TXEN on rising edge of RGMII[x]_TCLK and TXERR of falling edge of RGMII[x]_TCLK..

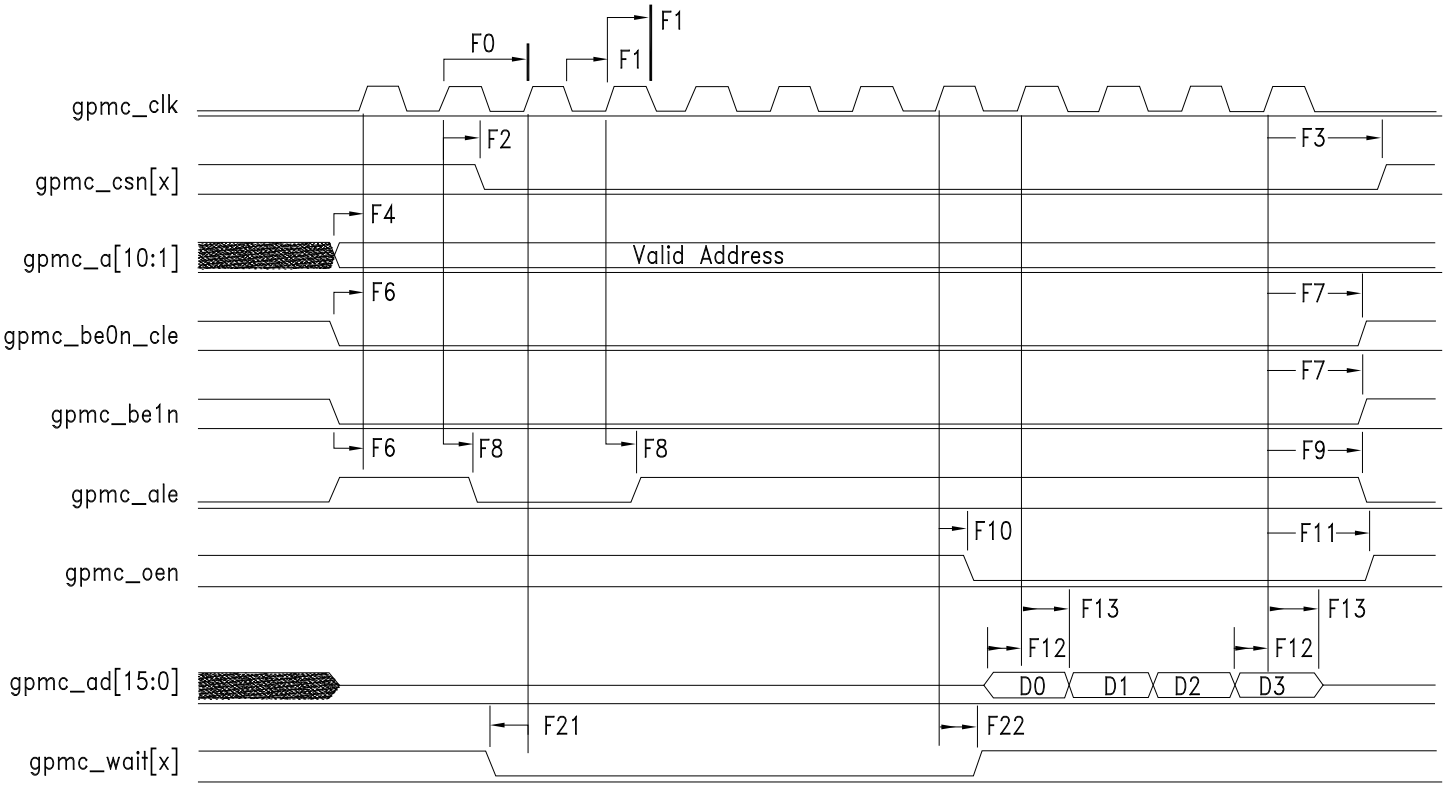
FIGURE 32. RGMII[x]_TD[3:0], RGMII[x]_TCTL Timing - RGMII Mode.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
B. In gpmc_wait[x], x is equal to 0 or 1.

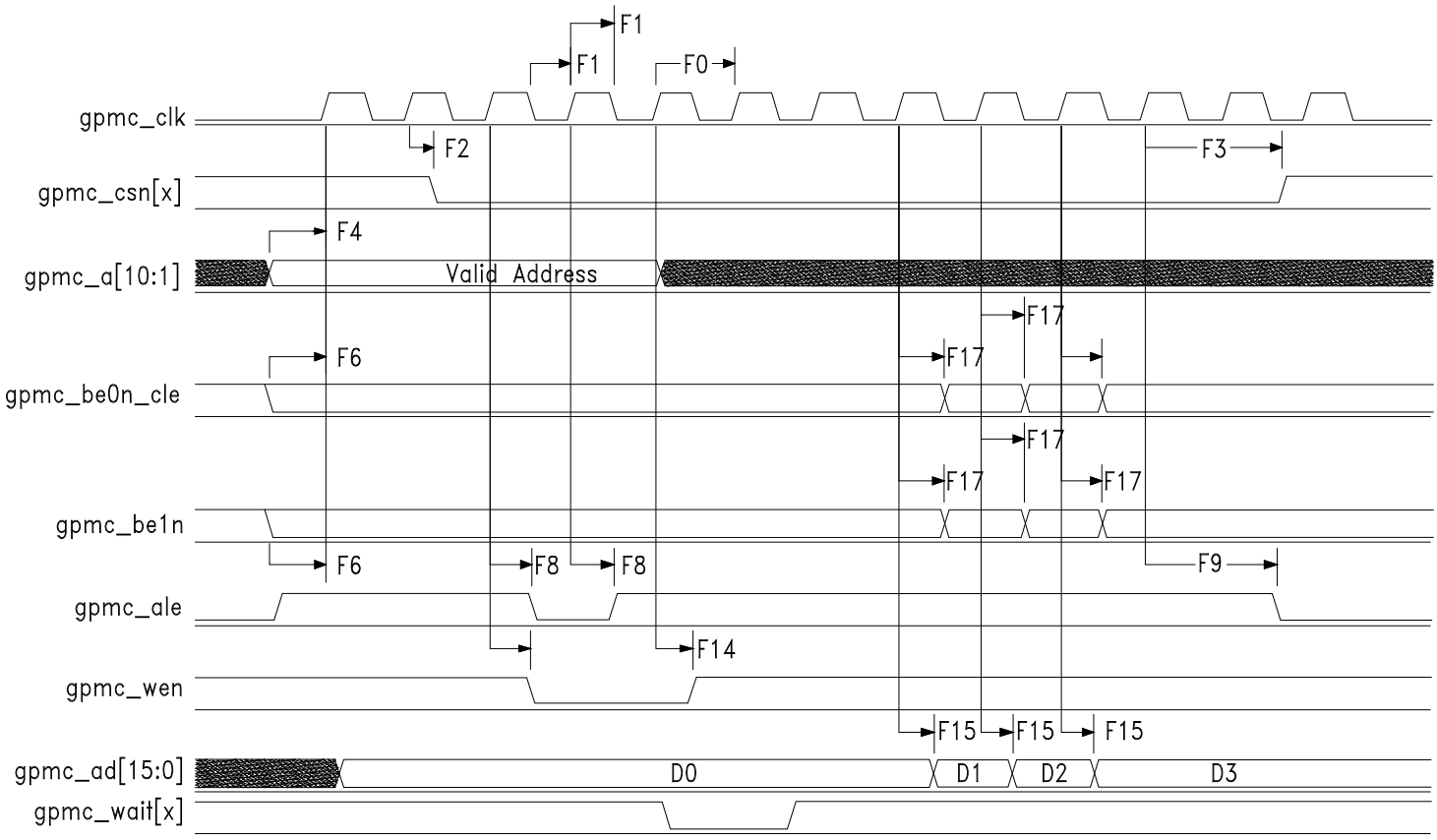
FIGURE 33. GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0).



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
B. In gpmc_wait[x], x is equal to 0 or 1.

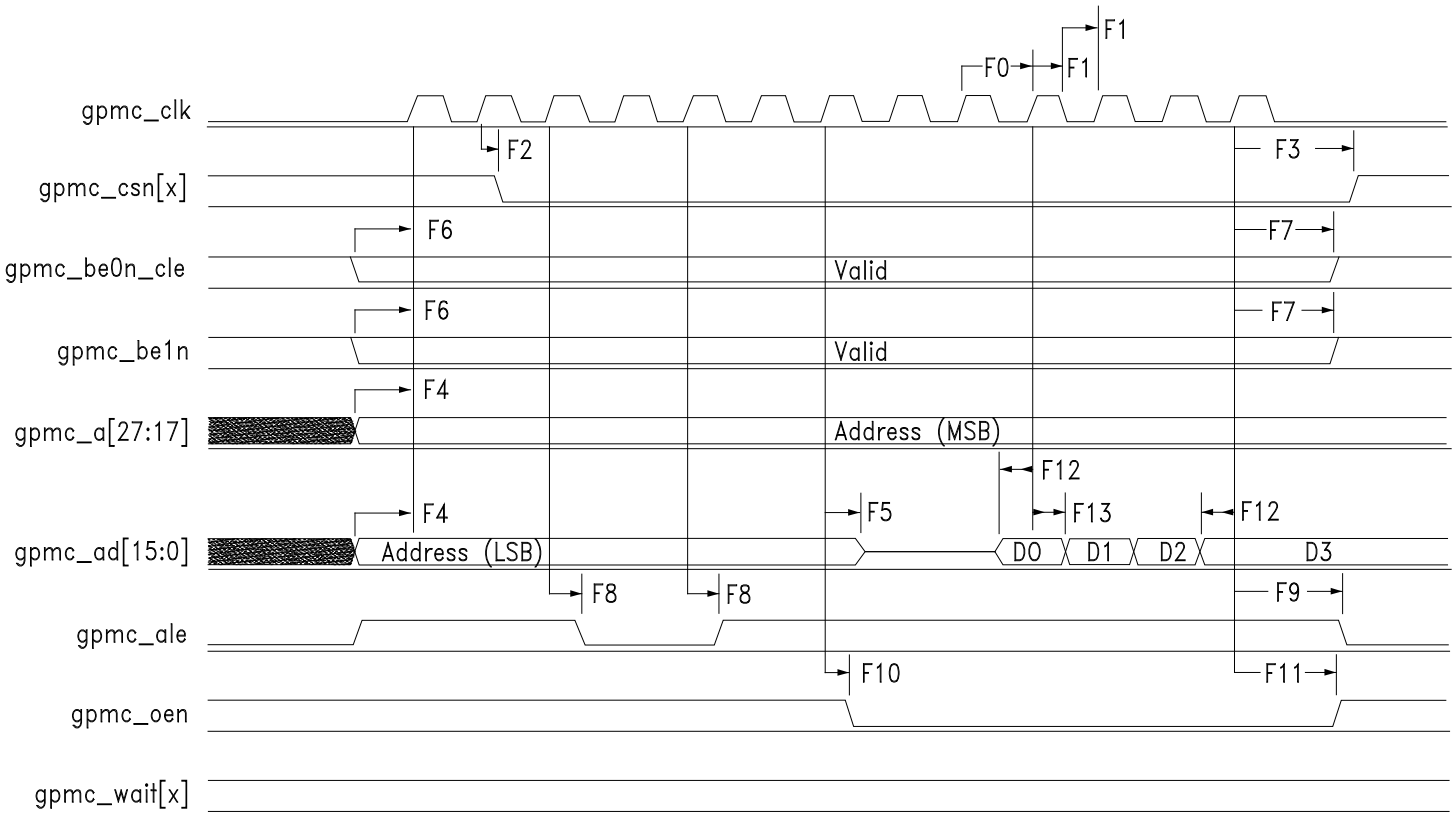
FIGURE 34. GPMC and NOR Flash—Synchronous Burst Read—4x16-bit (GpmcFCLKDivider = 0).



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
B. In gpmc_wait[x], x is equal to 0 or 1.

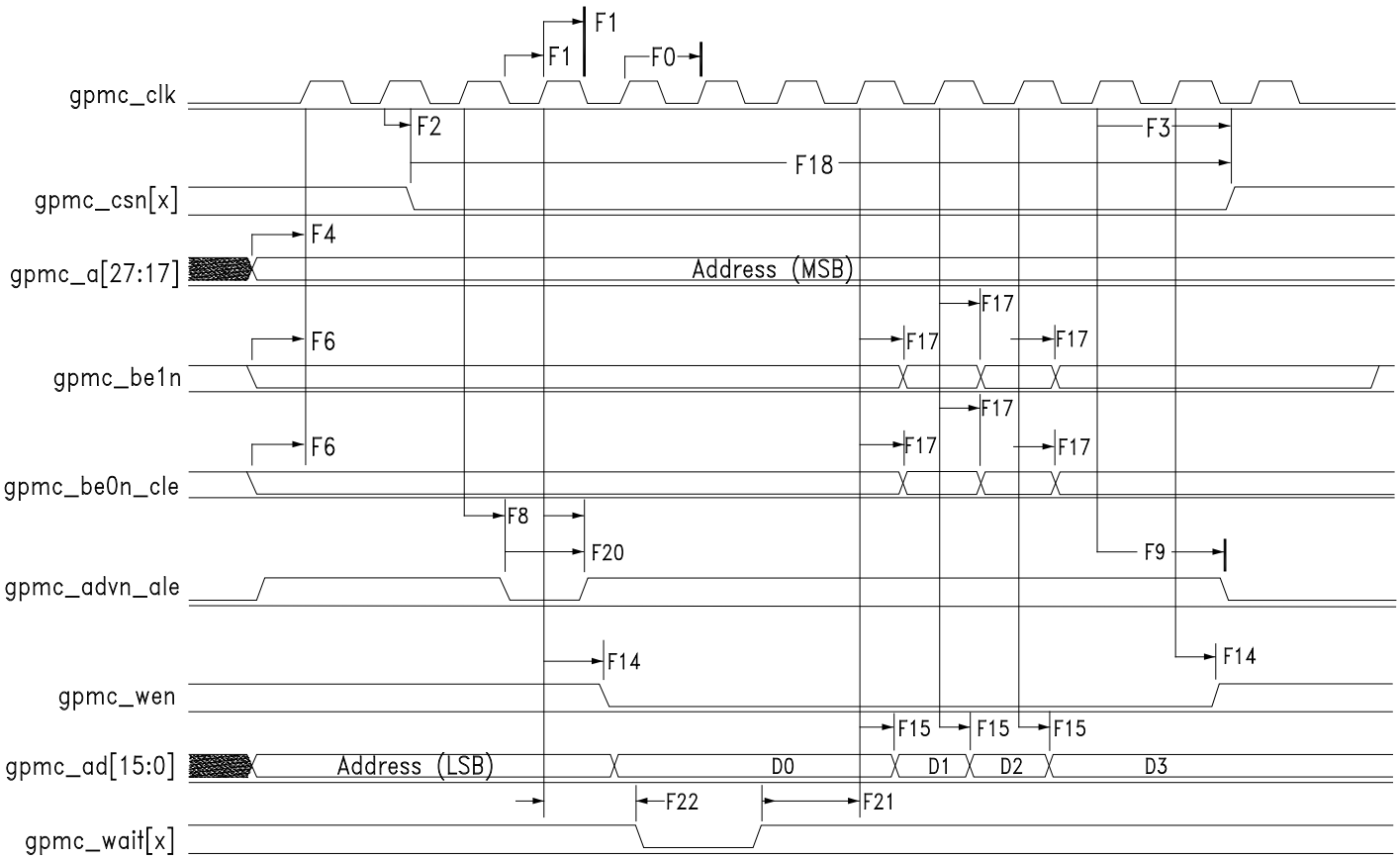
FIGURE 35. GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0).



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
B. In gpmc_wait[x], x is equal to 0 or 1.

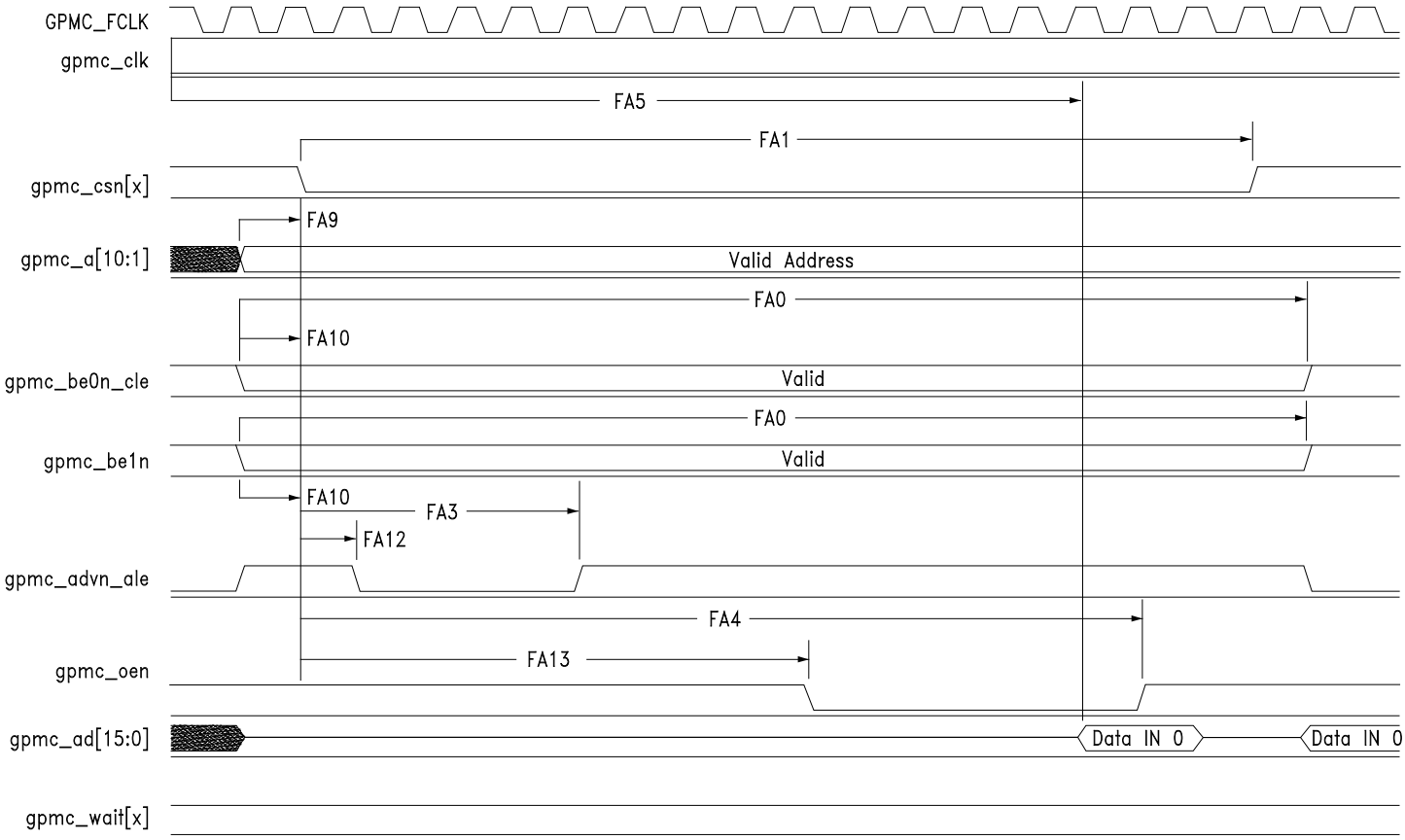
FIGURE 36. GPMC and Multiplexed NOR Flash—Synchronous Burst Read.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
B. In gpmc_wait[x], x is equal to 0 or 1.

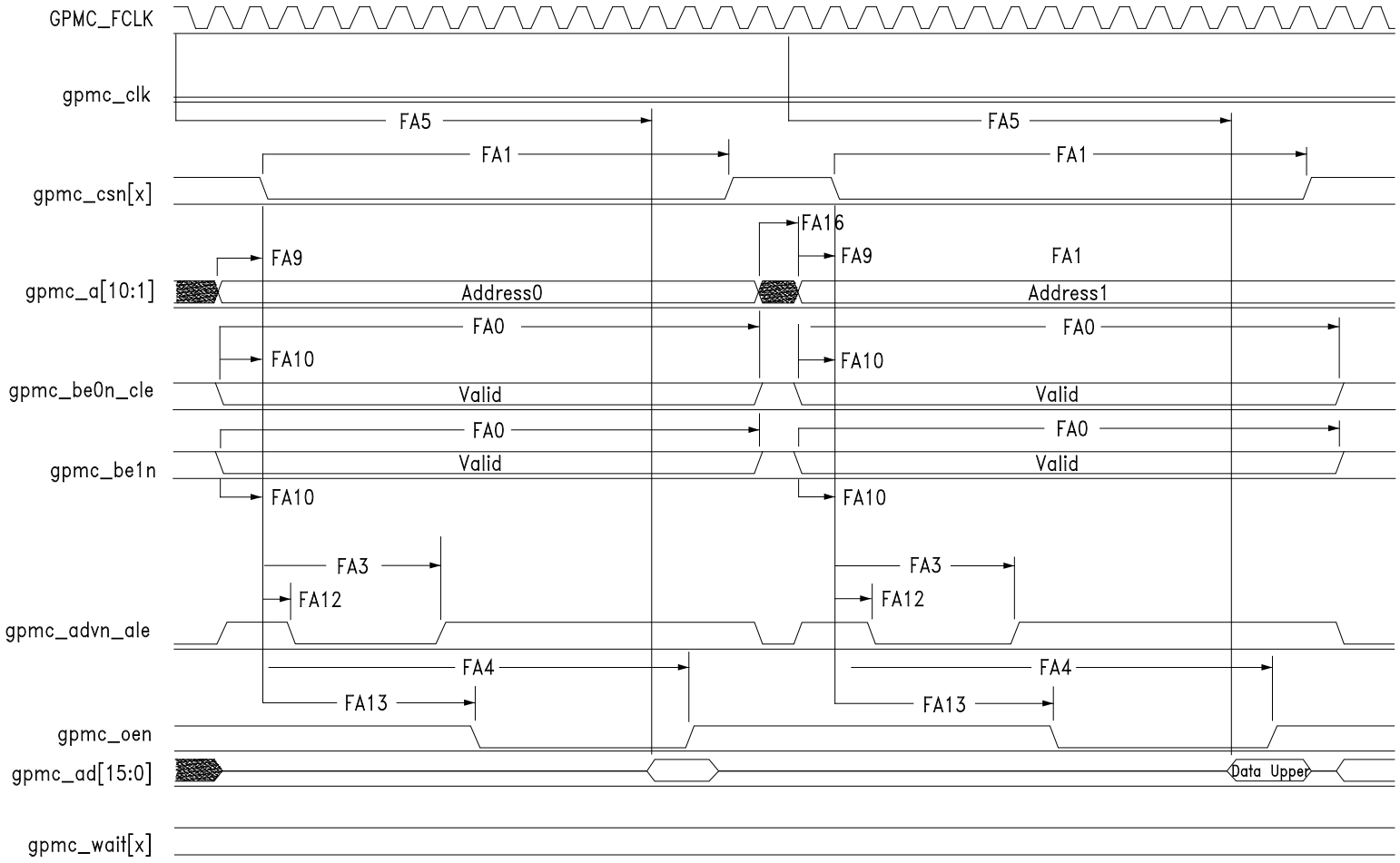
FIGURE 37. GPMC and Multiplexed NOR Flash—Synchronous Burst Write.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

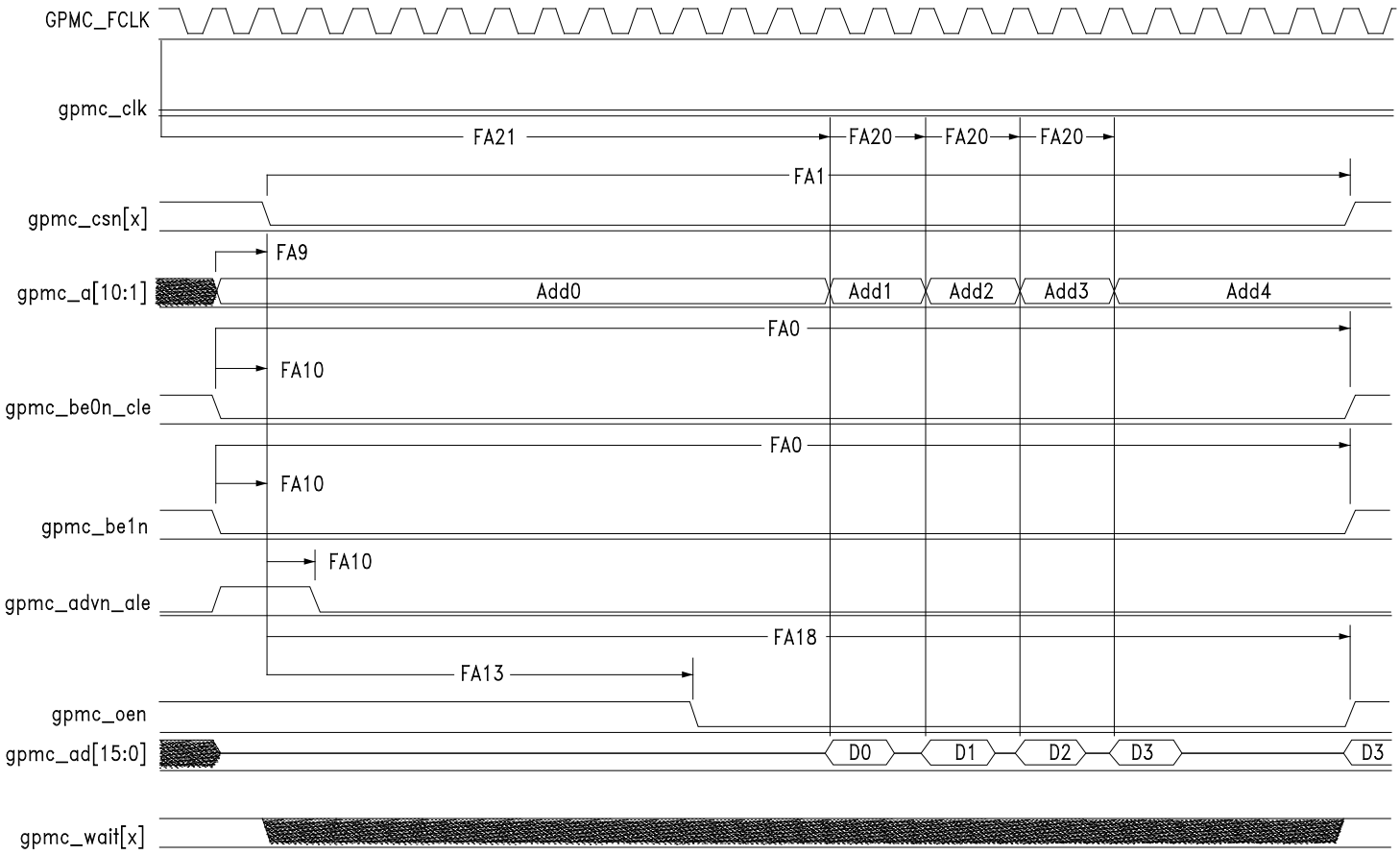
FIGURE 38. GPMC and NOR Flash—Asynchronous Read—Single Word.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

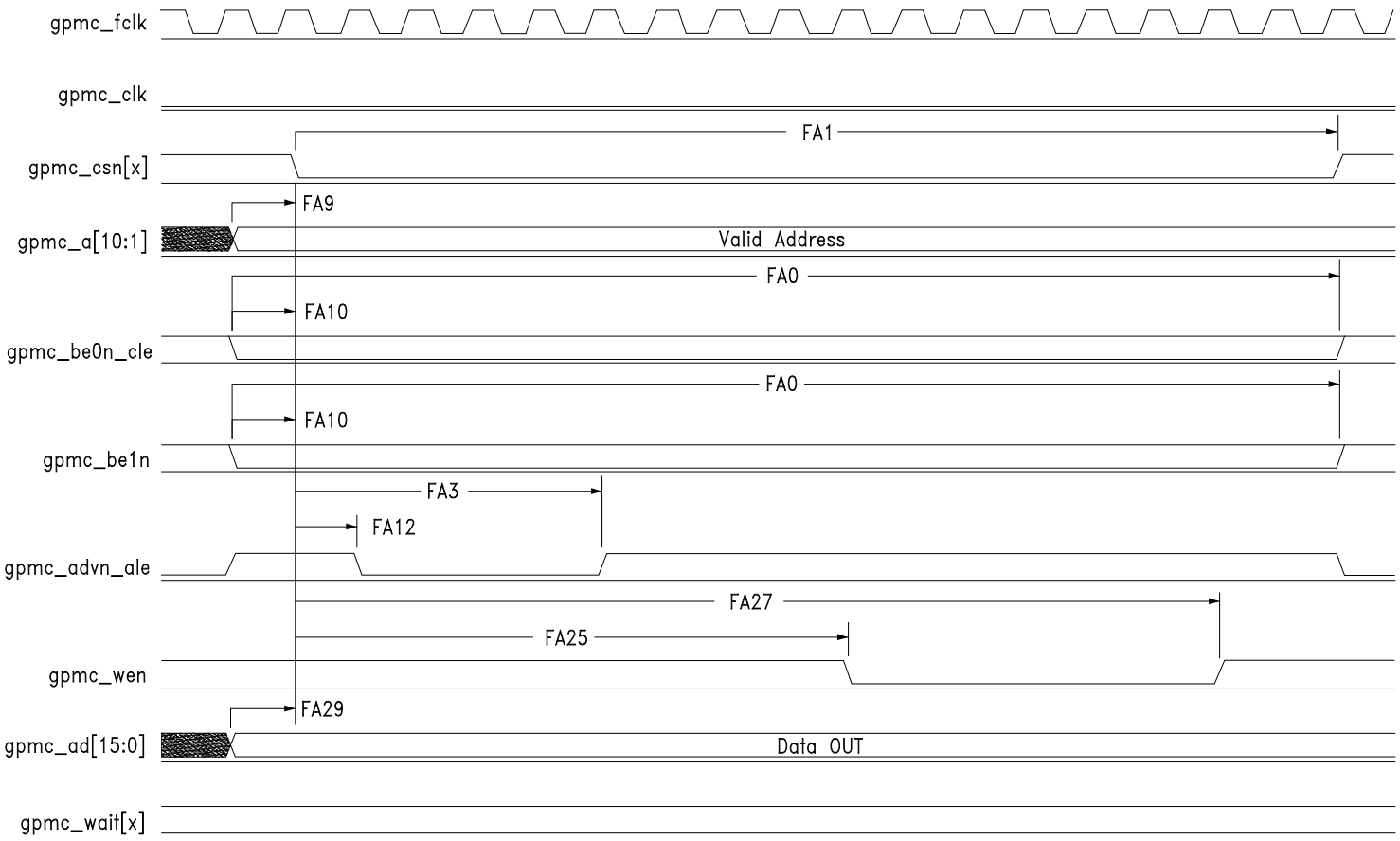
FIGURE 39. GPMC and NOR Flash—Asynchronous Read—32-bit.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

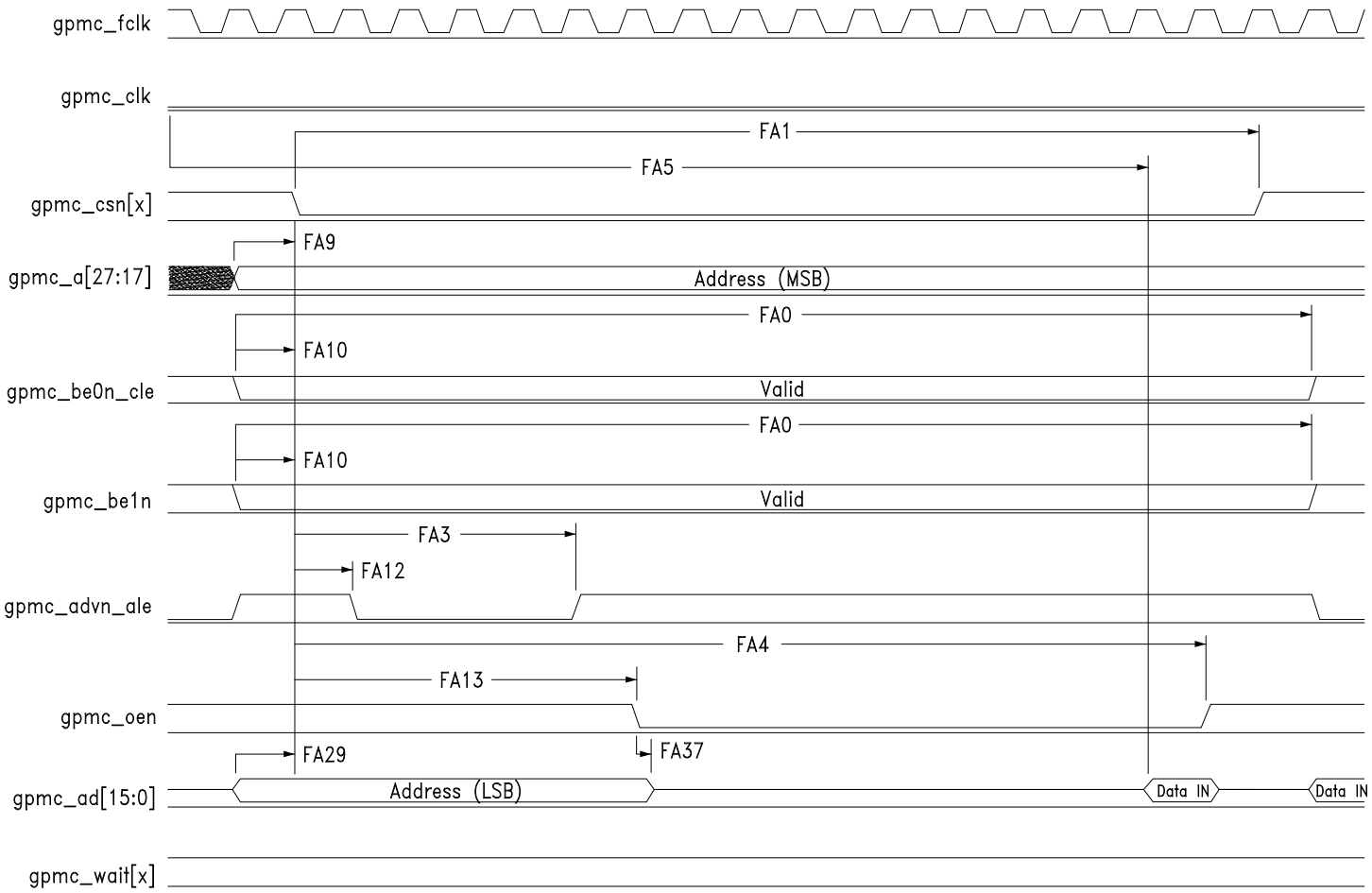
FIGURE 40. GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-bit.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.

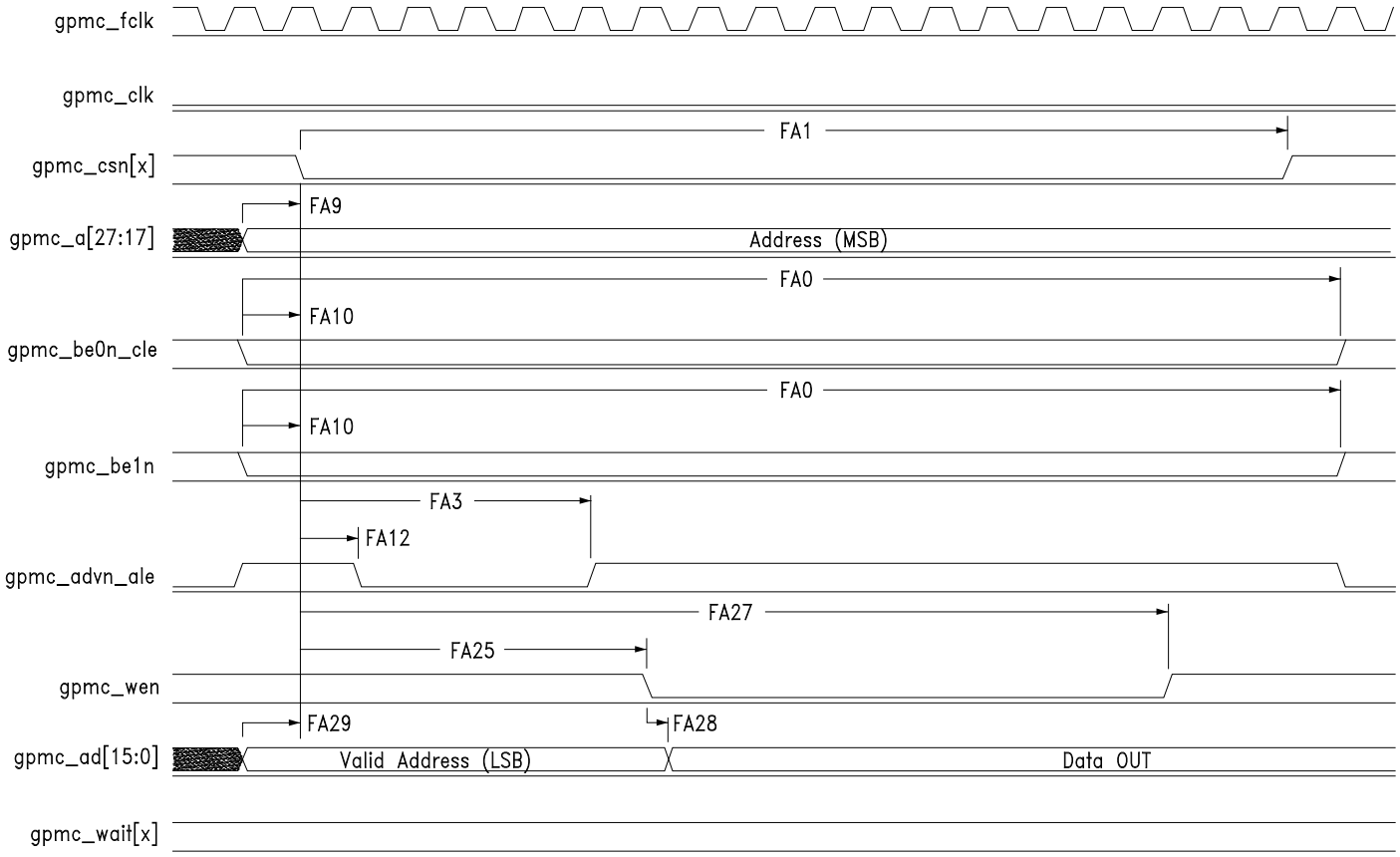
FIGURE 41. GPMC and NOR Flash—Asynchronous Write—Single Word.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

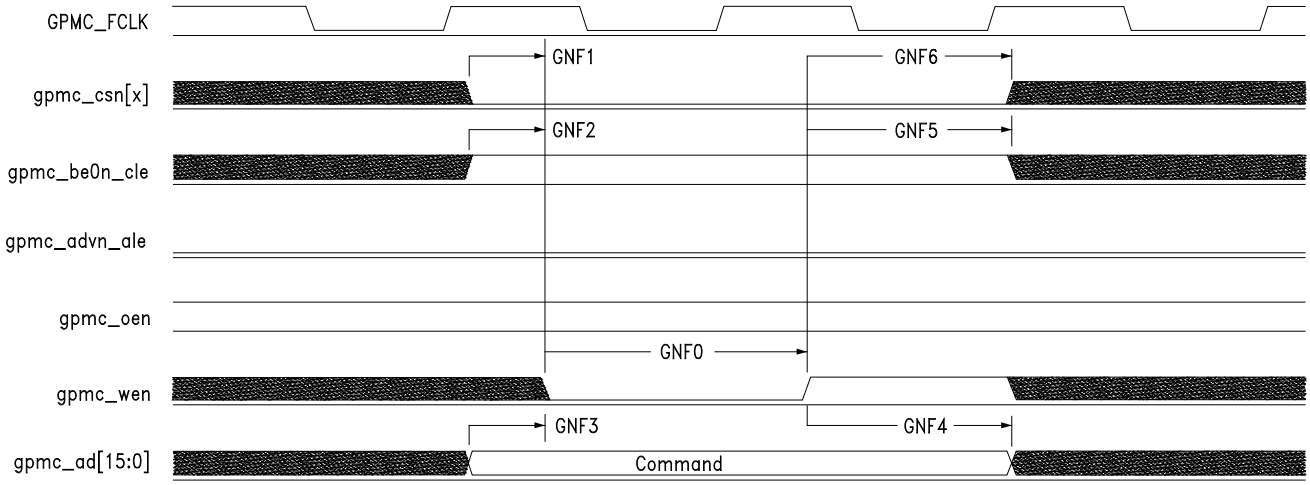
FIGURE 42. GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.

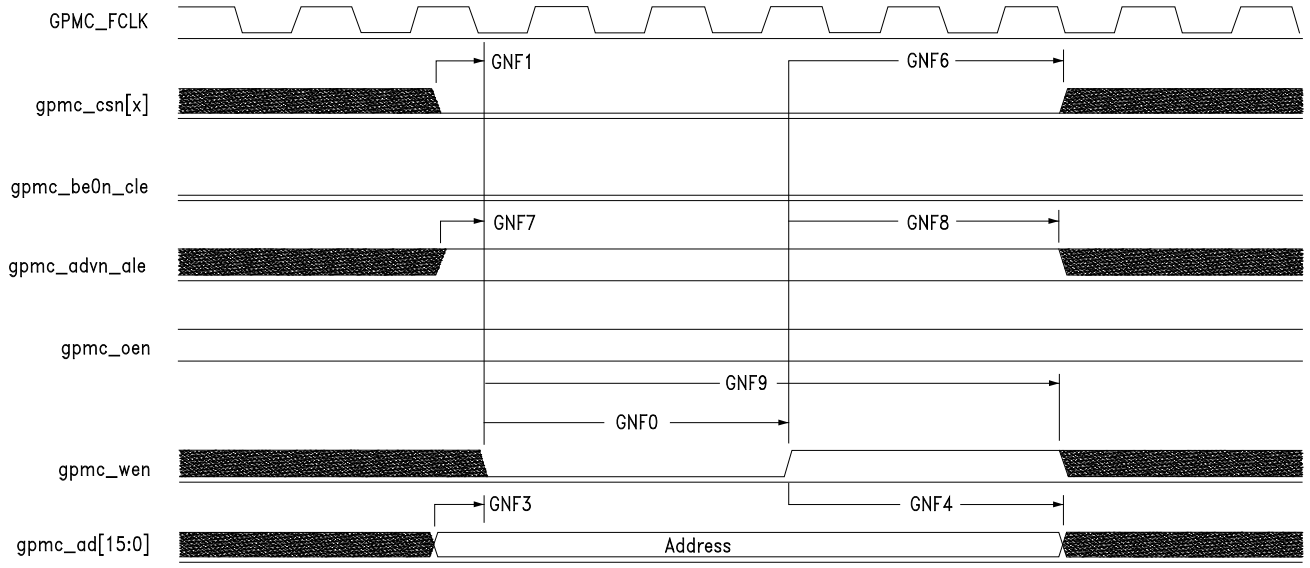
FIGURE 43. GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5..

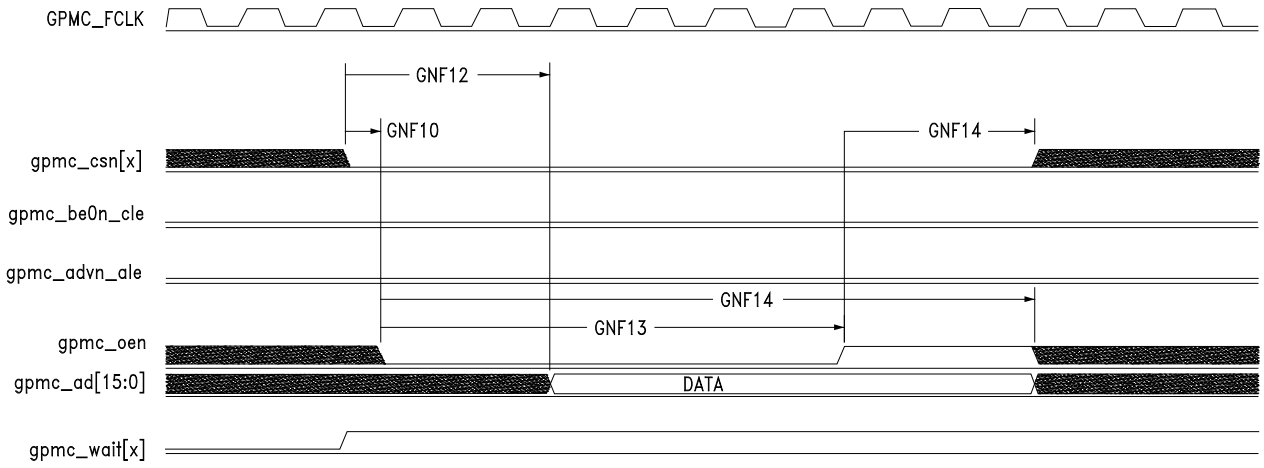
FIGURE 44. GPMC and NAND Flash—Command Latch Cycle.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5..

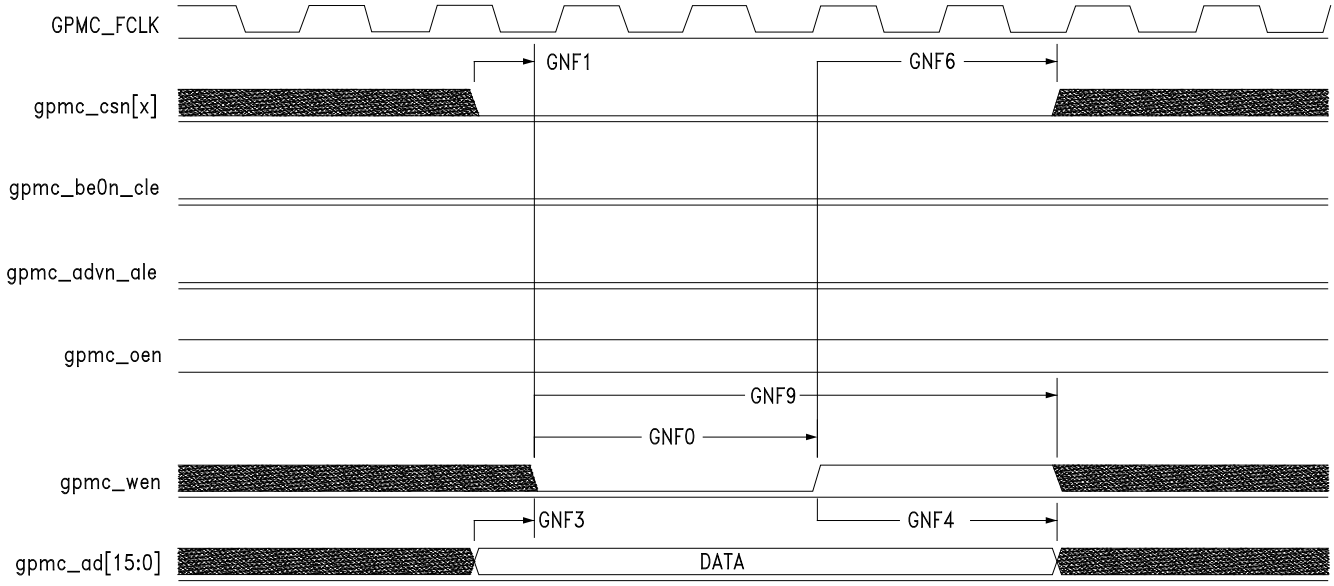
FIGURE 45. GPMC and NAND Flash—Address Latch Cycle.



Notes:

A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.

FIGURE 46. GPMC and NAND Flash—Data Read Cycle.



Notes:

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5..

FIGURE 47. GPMC and NAND Flash— Data Write Cycle.

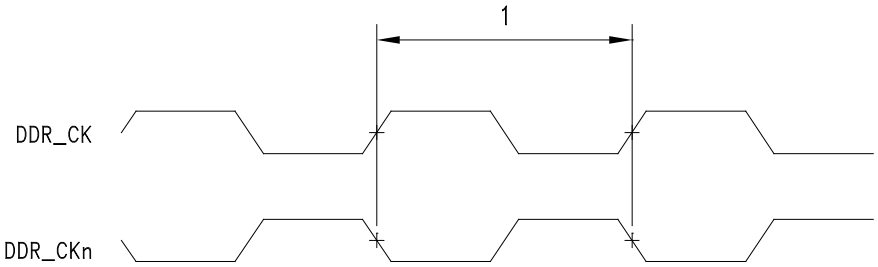


FIGURE 48. LPDDR Memory Interface Clock Timing.

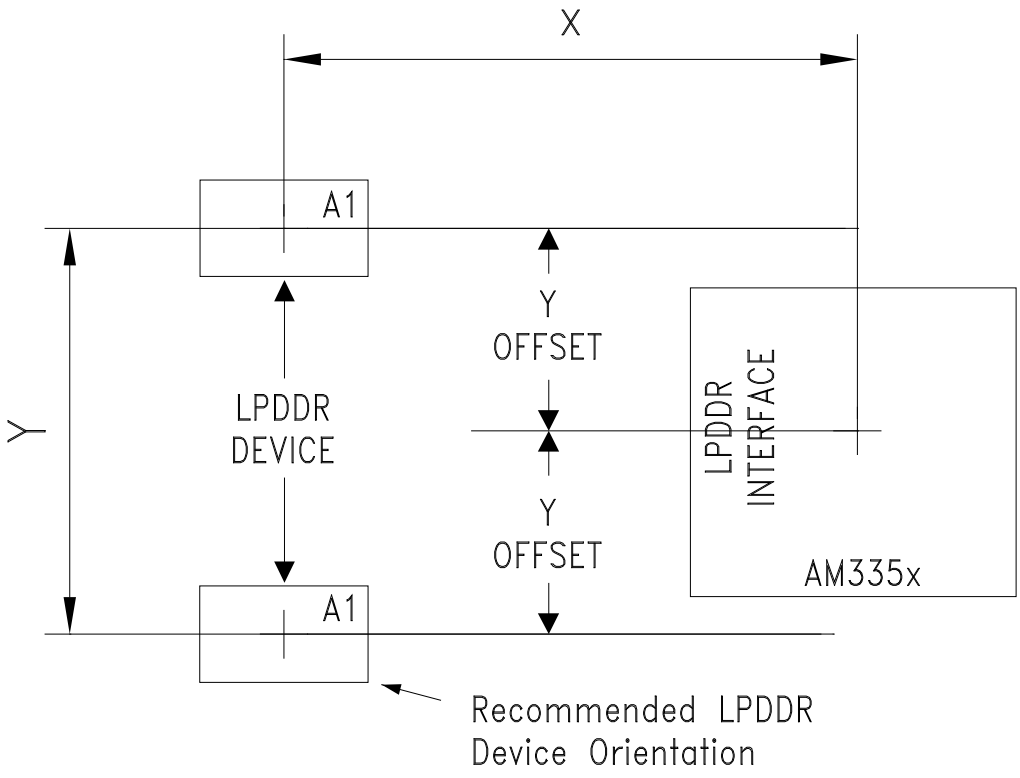


FIGURE 49. AM3358-EP Device and LPDDR Device Placement.

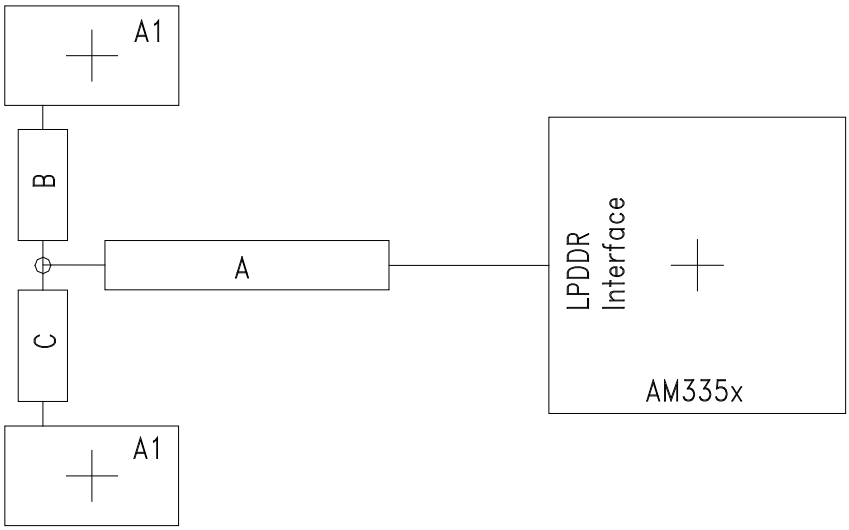


FIGURE 50. CK and ADDR_CTRL Routing and Topology.

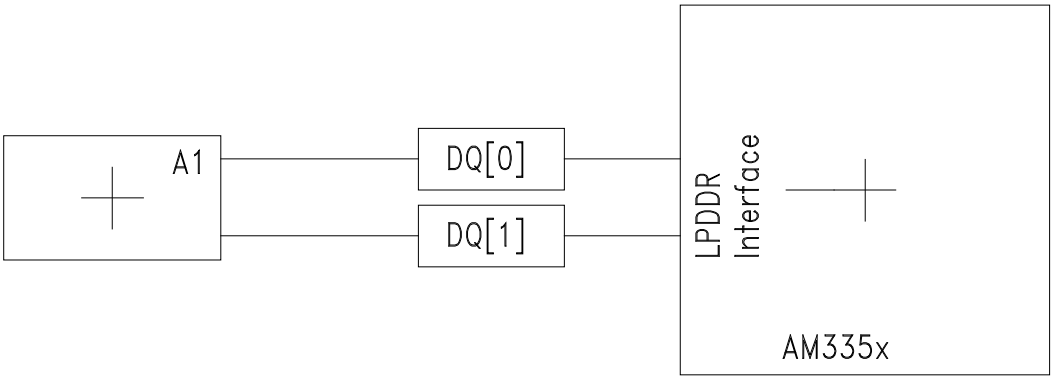


FIGURE 51. DQS[x] and DQ[x] Routing and Topology.

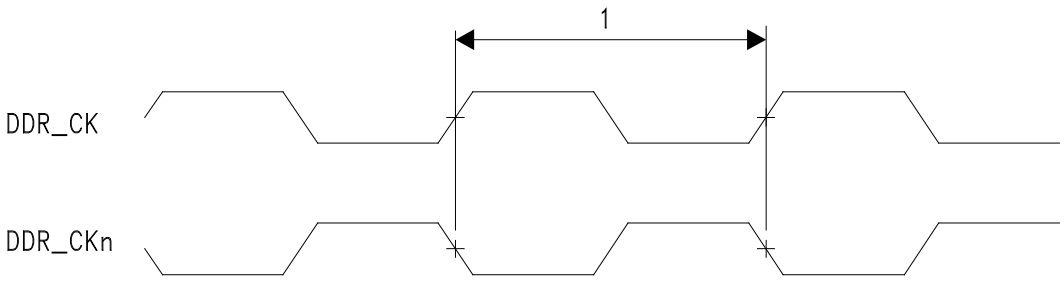


FIGURE 52. DDR2 Memory Interface Clock Timing.

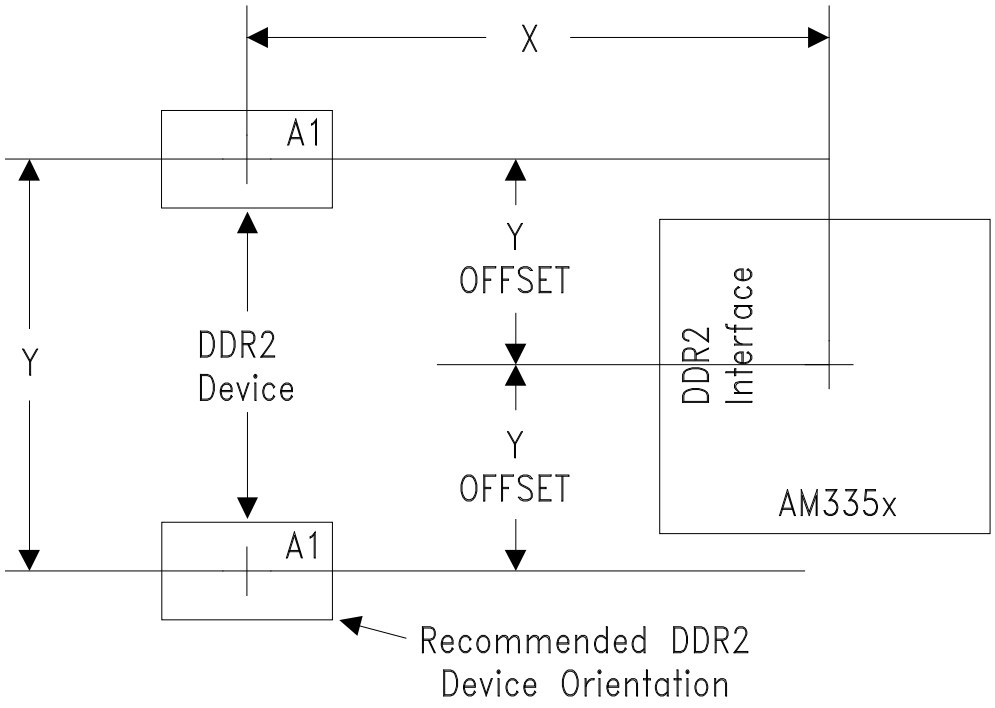


FIGURE 53. AM3358-EP Device and DDR2 Device Placement.

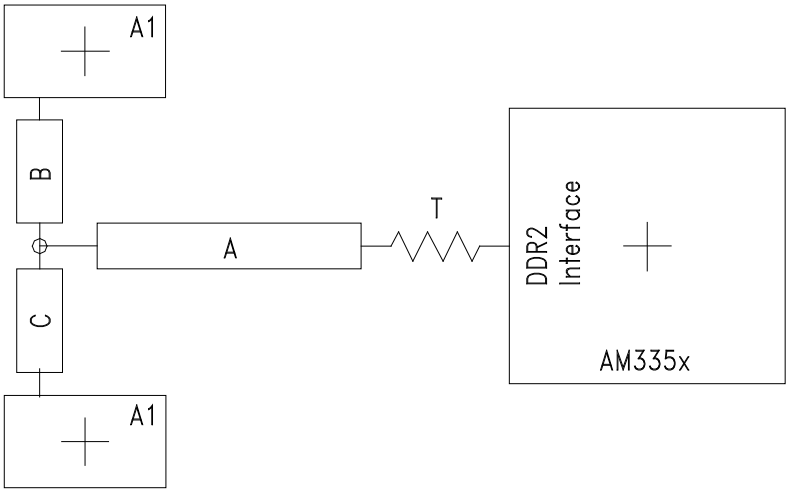


FIGURE 54. CK and ADDR_CTRL Routing and Topology.

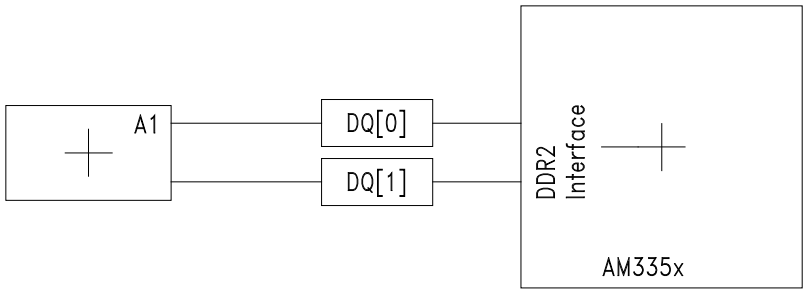


FIGURE 55. DQS[x] and DQ[x] Routing and Topology.

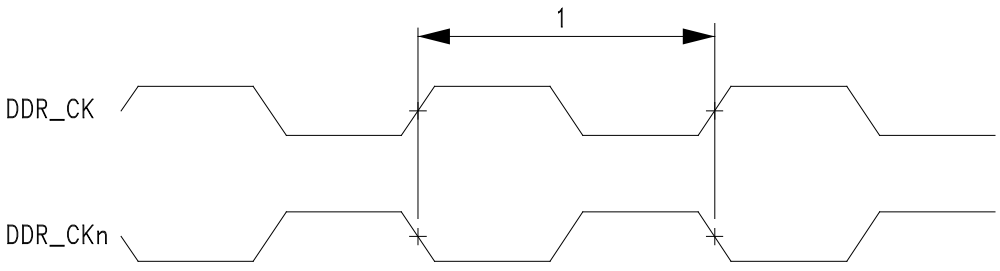


FIGURE 56. DDR3 Memory Interface Clock Timing.

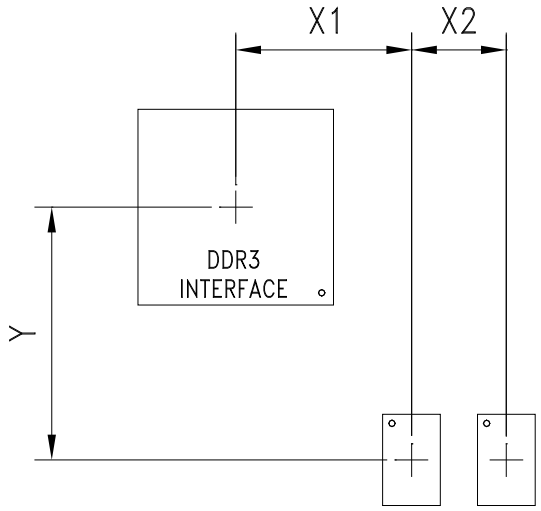


FIGURE 57. Placement Specifications.

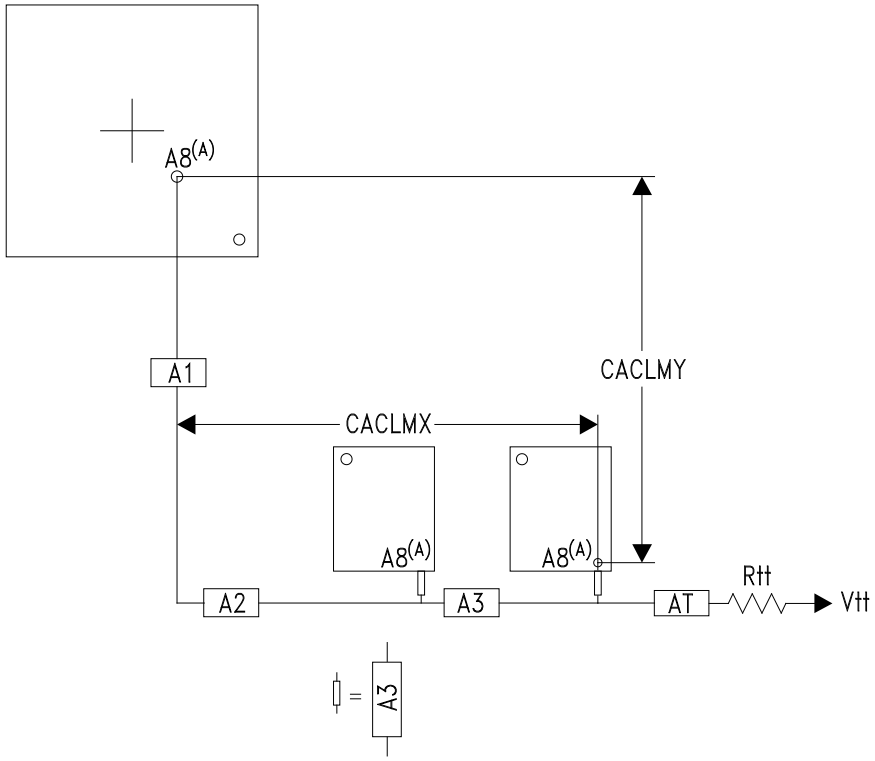
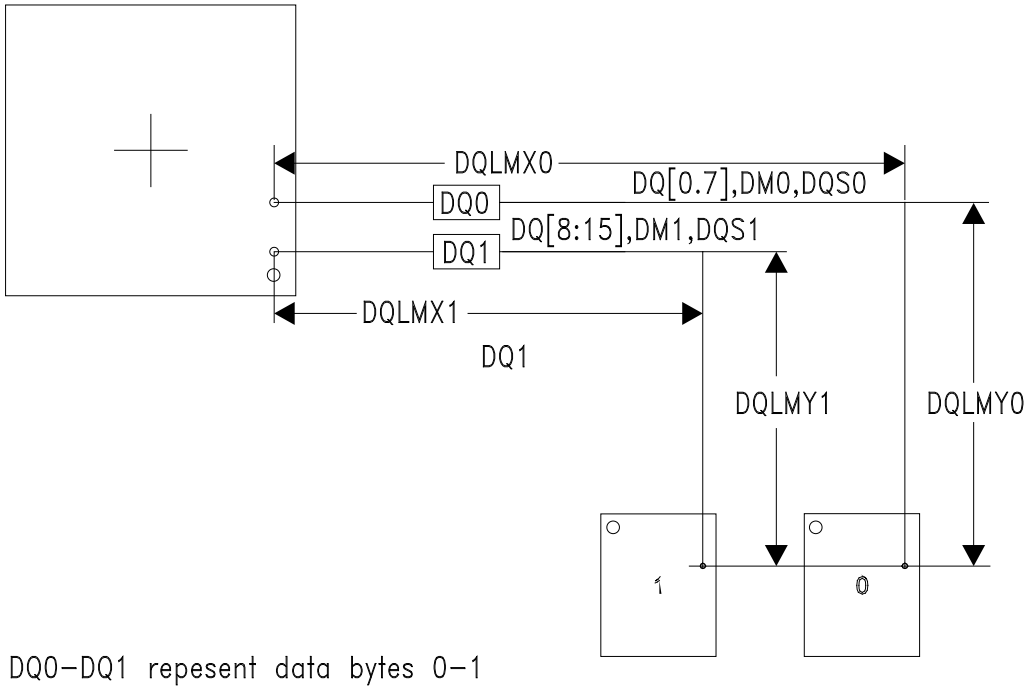


FIGURE 58. CLM for Two Address Loads on One Side of PCB.



Notes:

There are two DQLMs, one for each byte (16-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:
DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1

FIGURE 59. DQLM for Any Number of Allowed DDR3 Devices.

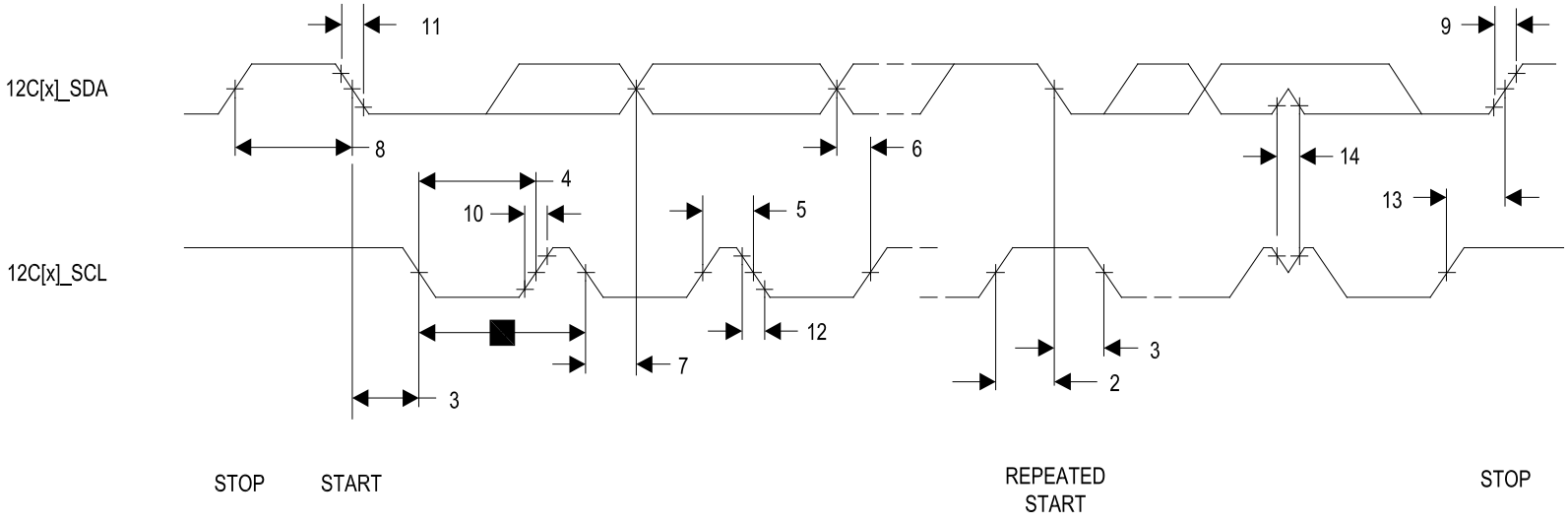


FIGURE 60. I²C Receive Timing.

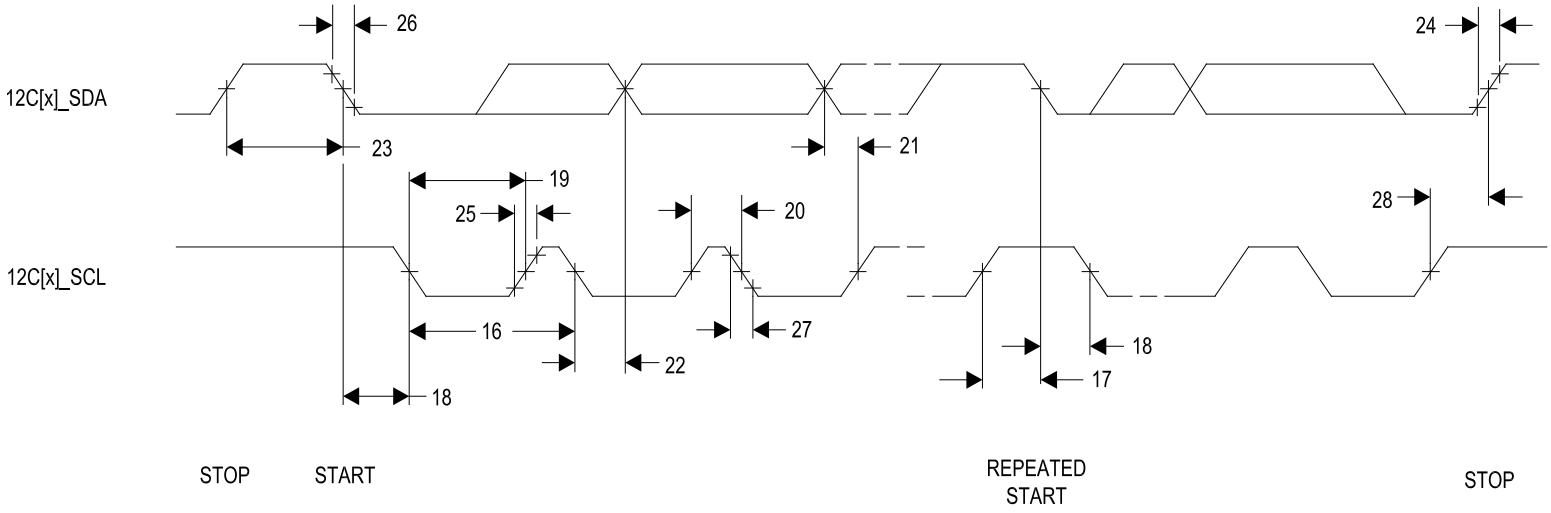


FIGURE 61. I²C Transmit Timing.

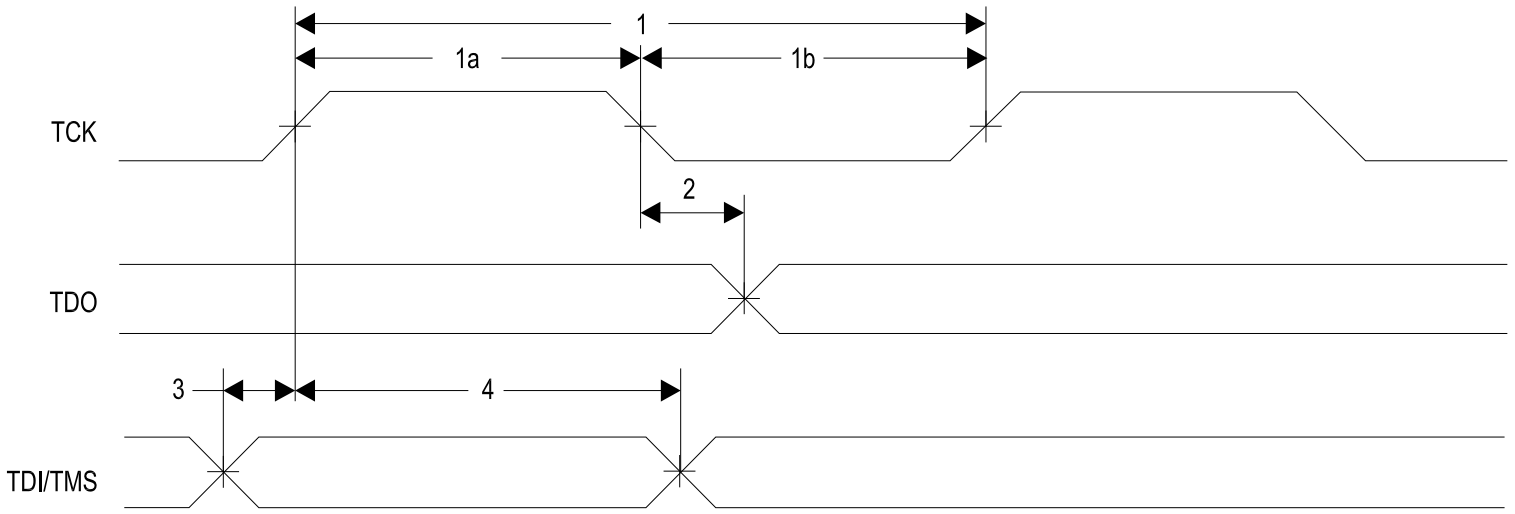
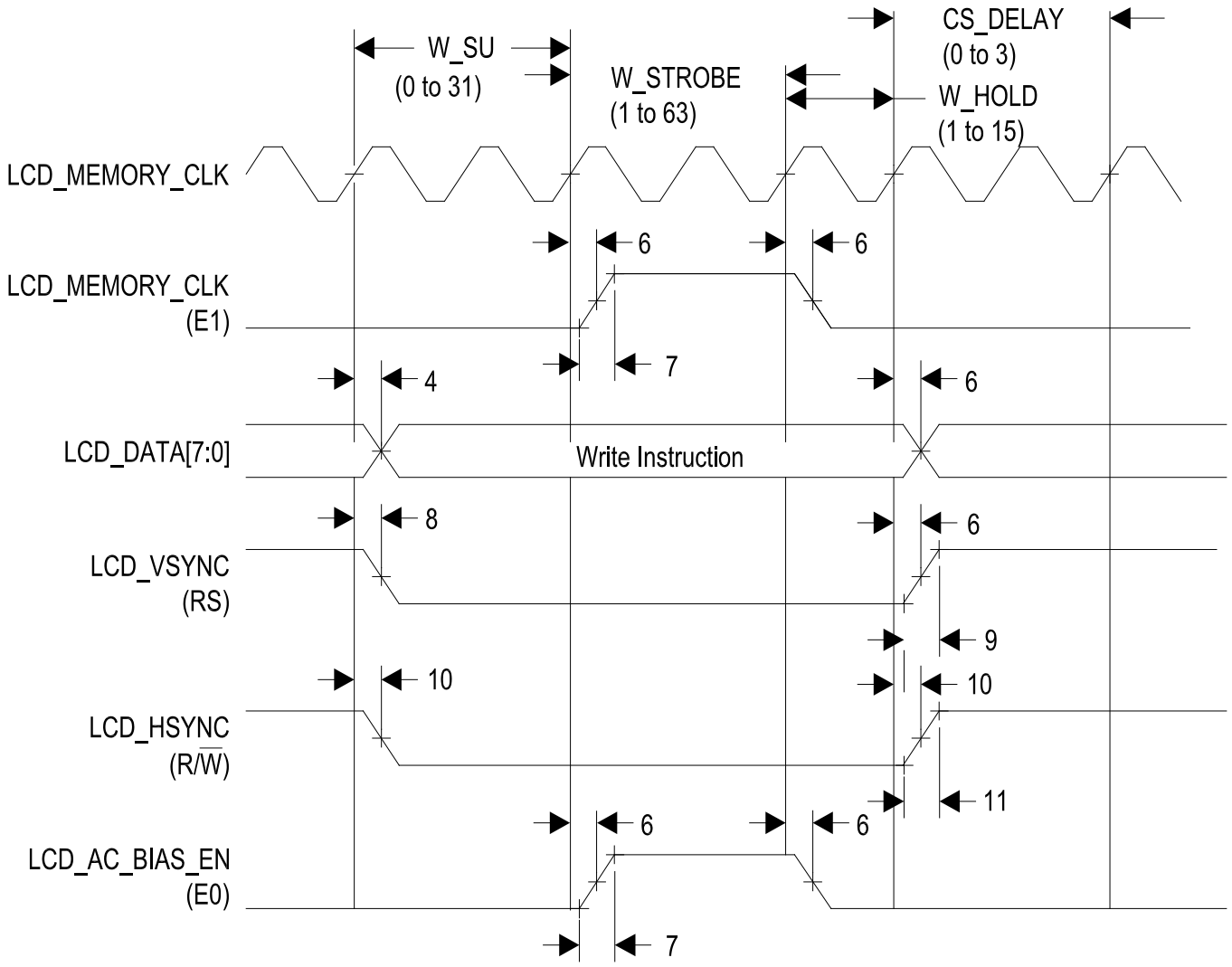


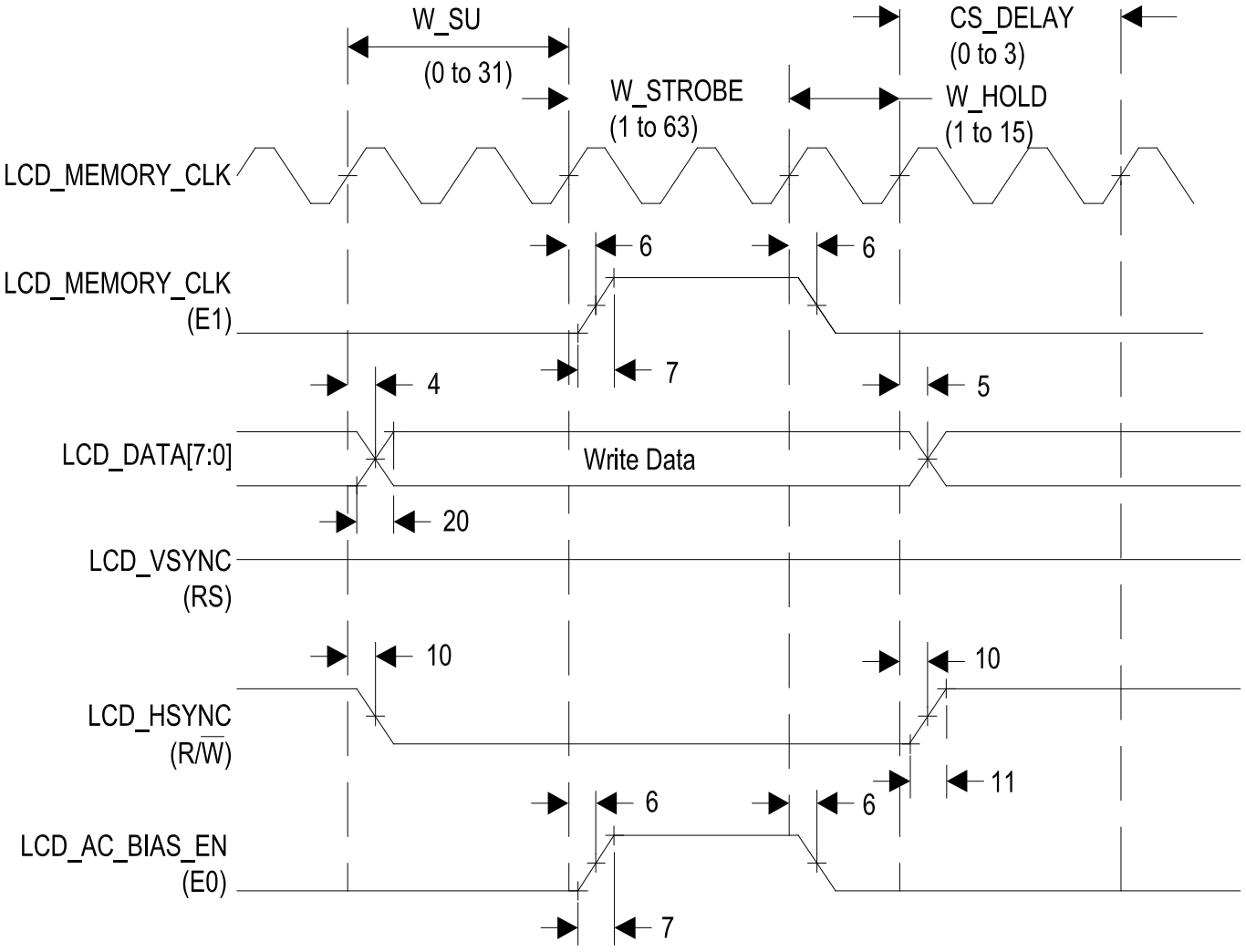
FIGURE 62. JTAG Timing.



Notes:

A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK waveform is only shown as a reference of the internal clock that sequences the other signals. The second LCD_MEMORY_CLK waveform is shown as E1 since the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

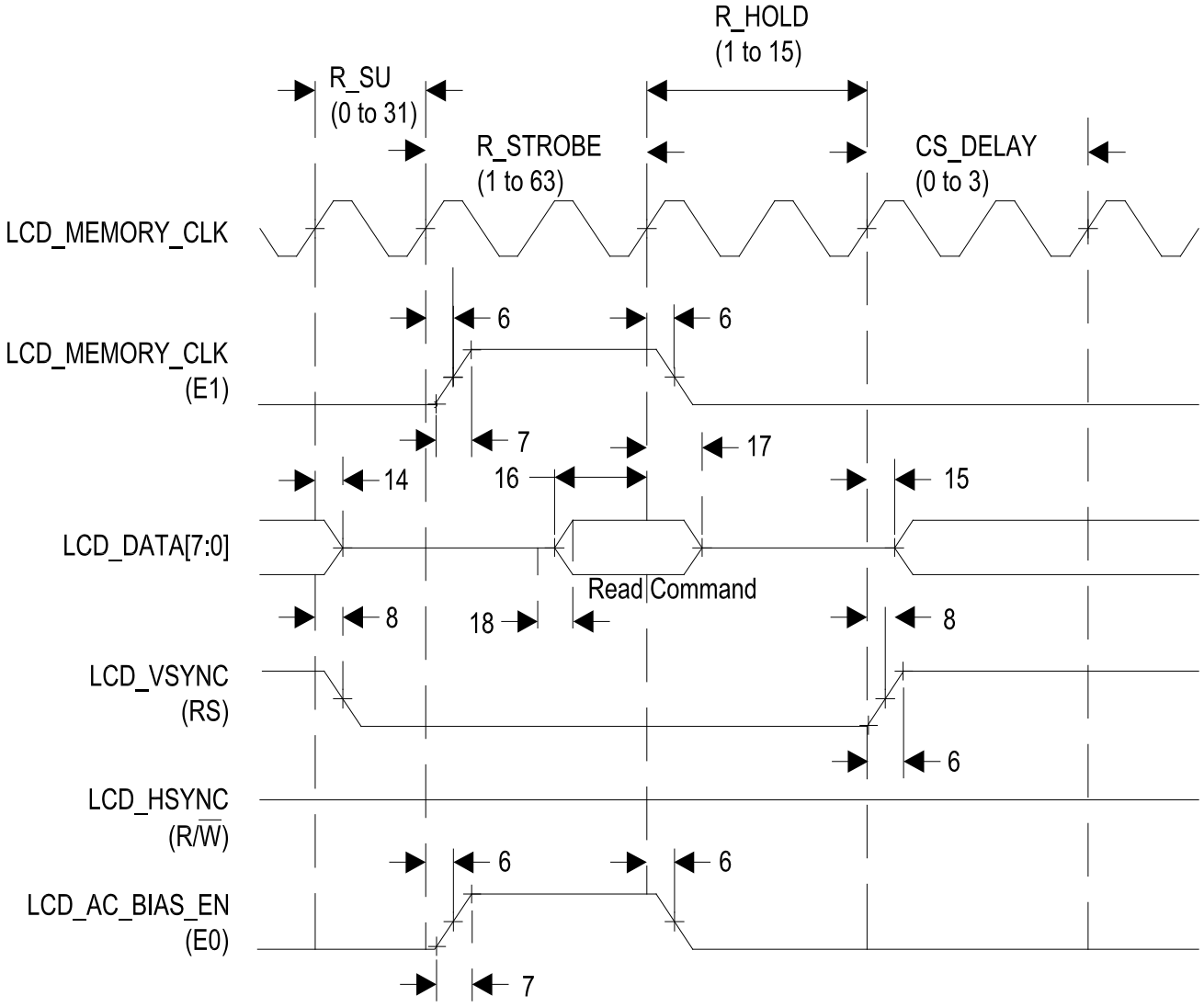
FIGURE 63. Command Write in Hitachi Mode.



Notes:

A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK wavefor m is only shown as a reference of the internal clock that sequences the other signals.The second LCD_MEMORY_CLK waveform is shown as E1 since the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

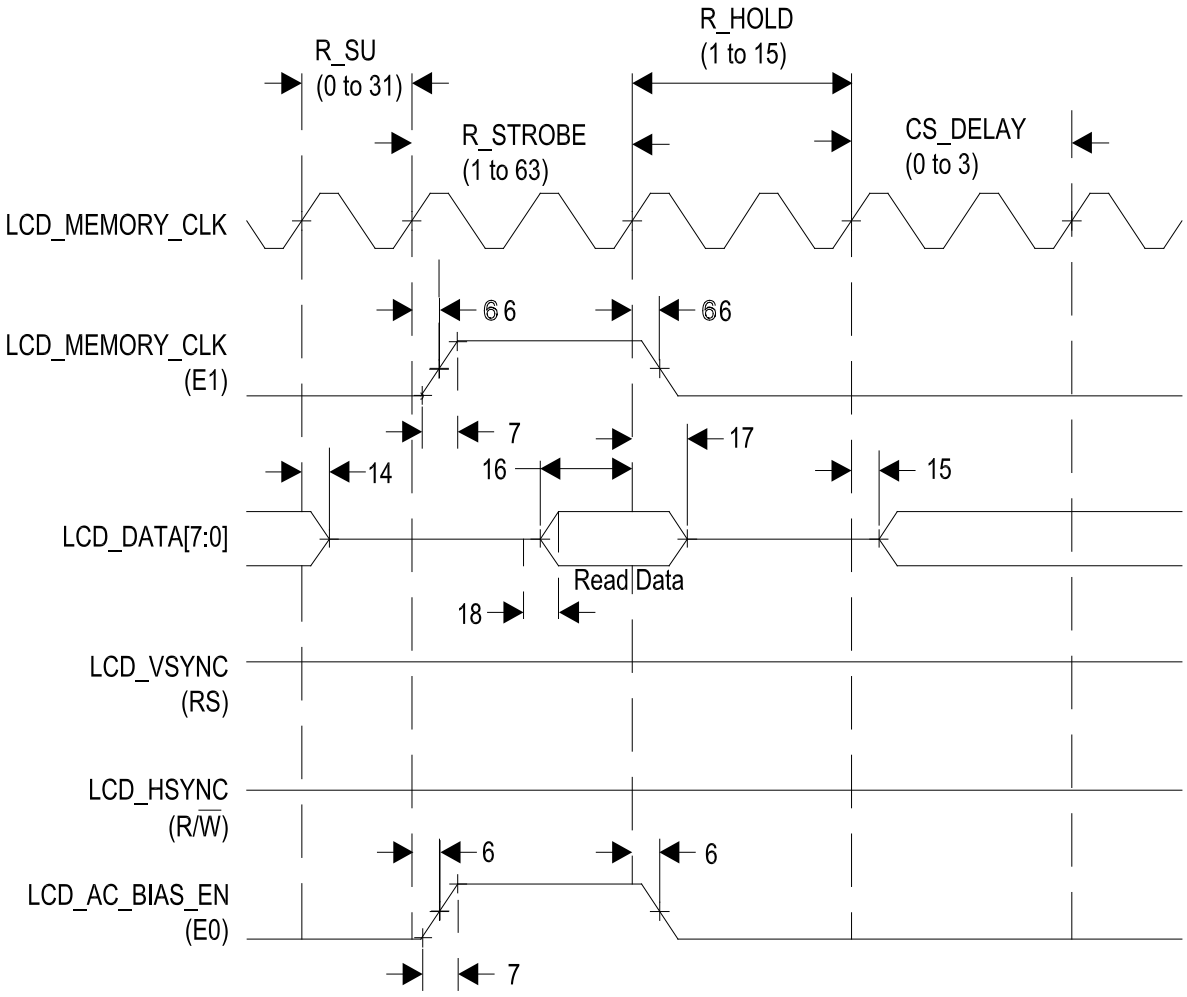
FIGURE 64. Data Write in Hitachi Mode.



Notes:

A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK waveform is only shown as a reference of the internal clock that sequences the other signals. The second LCD_MEMORY_CLK waveform is shown as E1 since the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

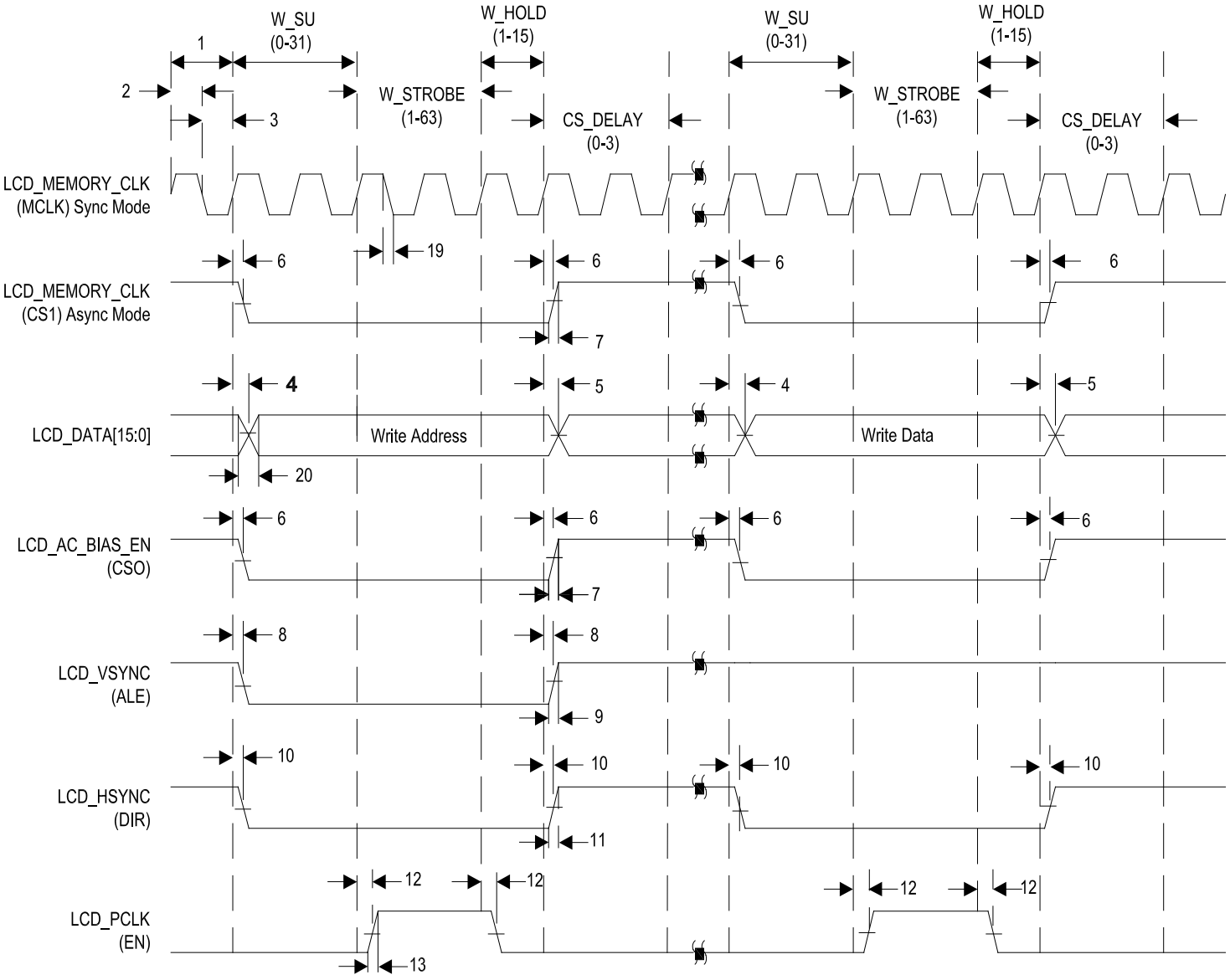
FIGURE 65. Command Read in Hitachi Mode.



Notes:

A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK waveform is only shown as a reference of the internal clock that sequences the other signals. The second LCD_MEMORY_CLK waveform is shown as E1 since the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

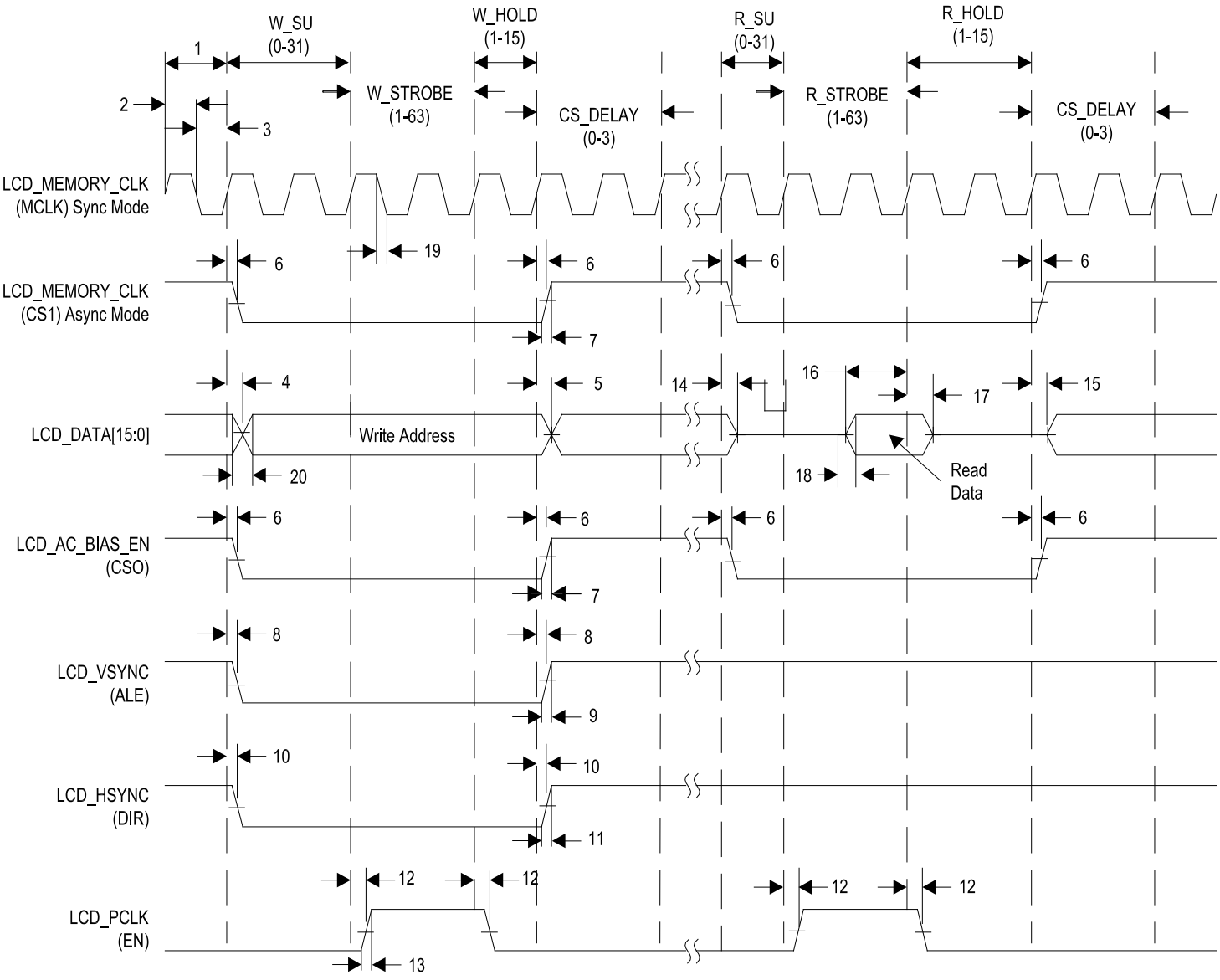
FIGURE 66. Data Read in Hitachi Mode.



Notes:

A. Motorola mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals..

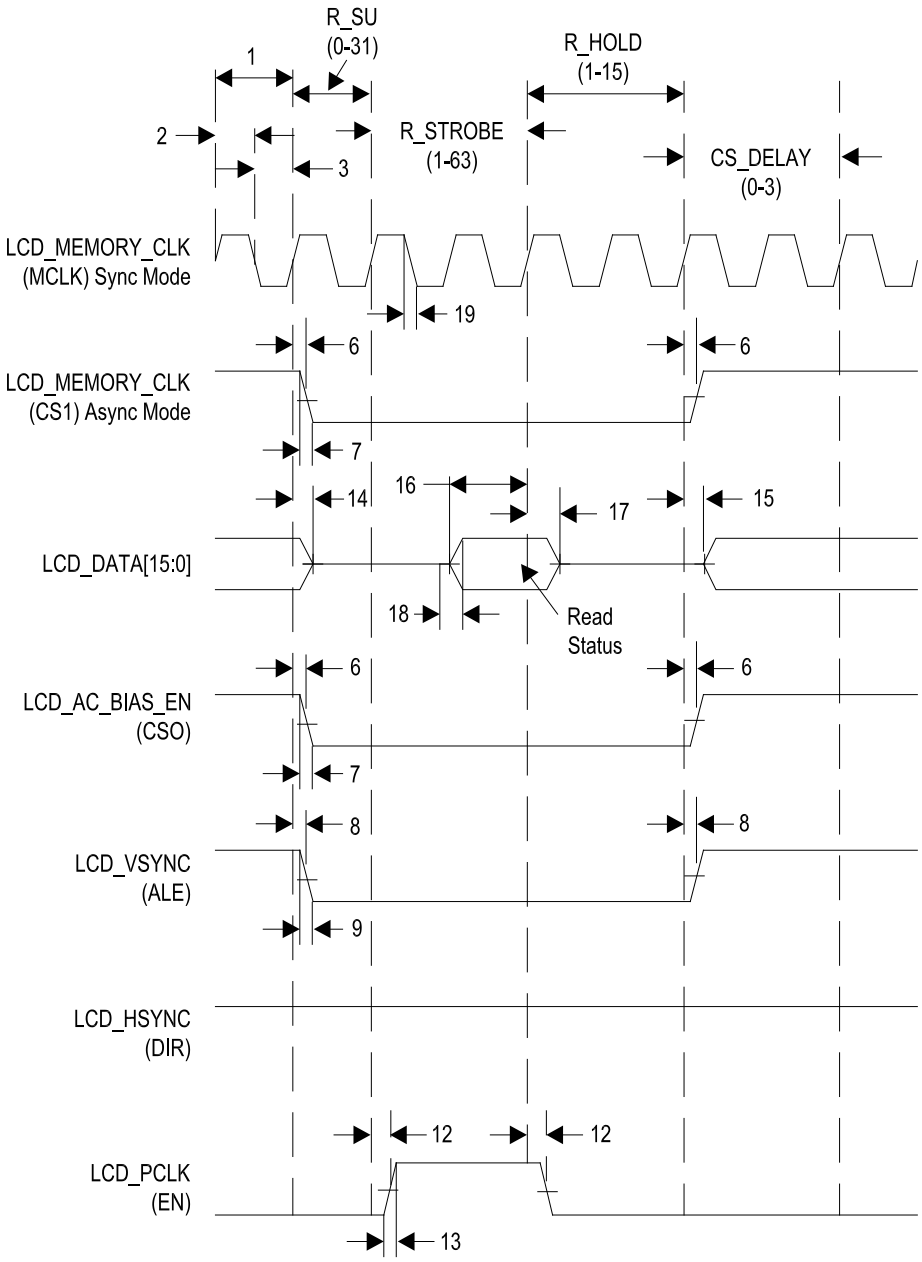
FIGURE 67. Micro-Interface Graphic Display Motorola Write.



Notes:

A. Motorola mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

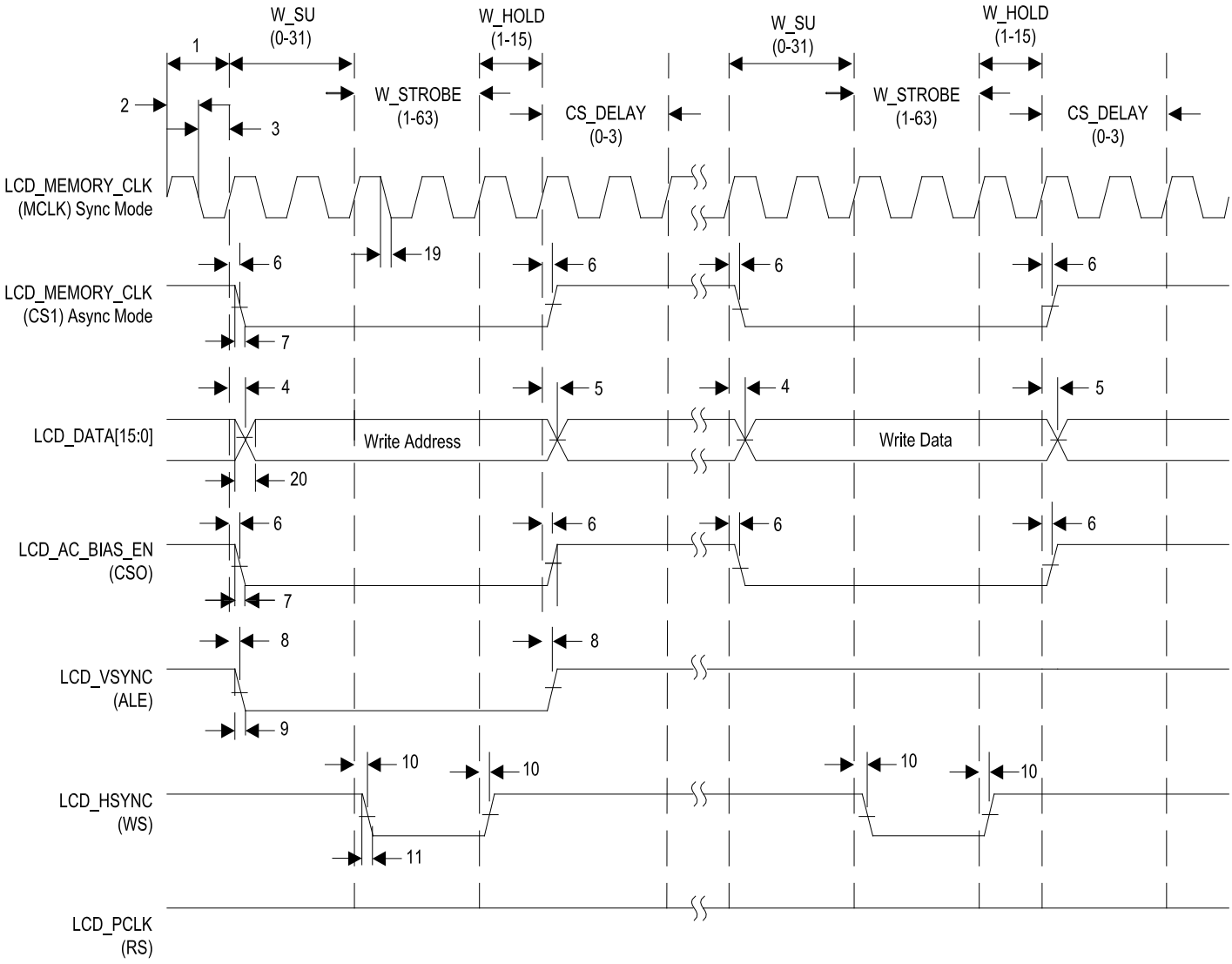
FIGURE 68. Micro-Interface Graphic Display Motorola Read.



Notes:

A. Motorola mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

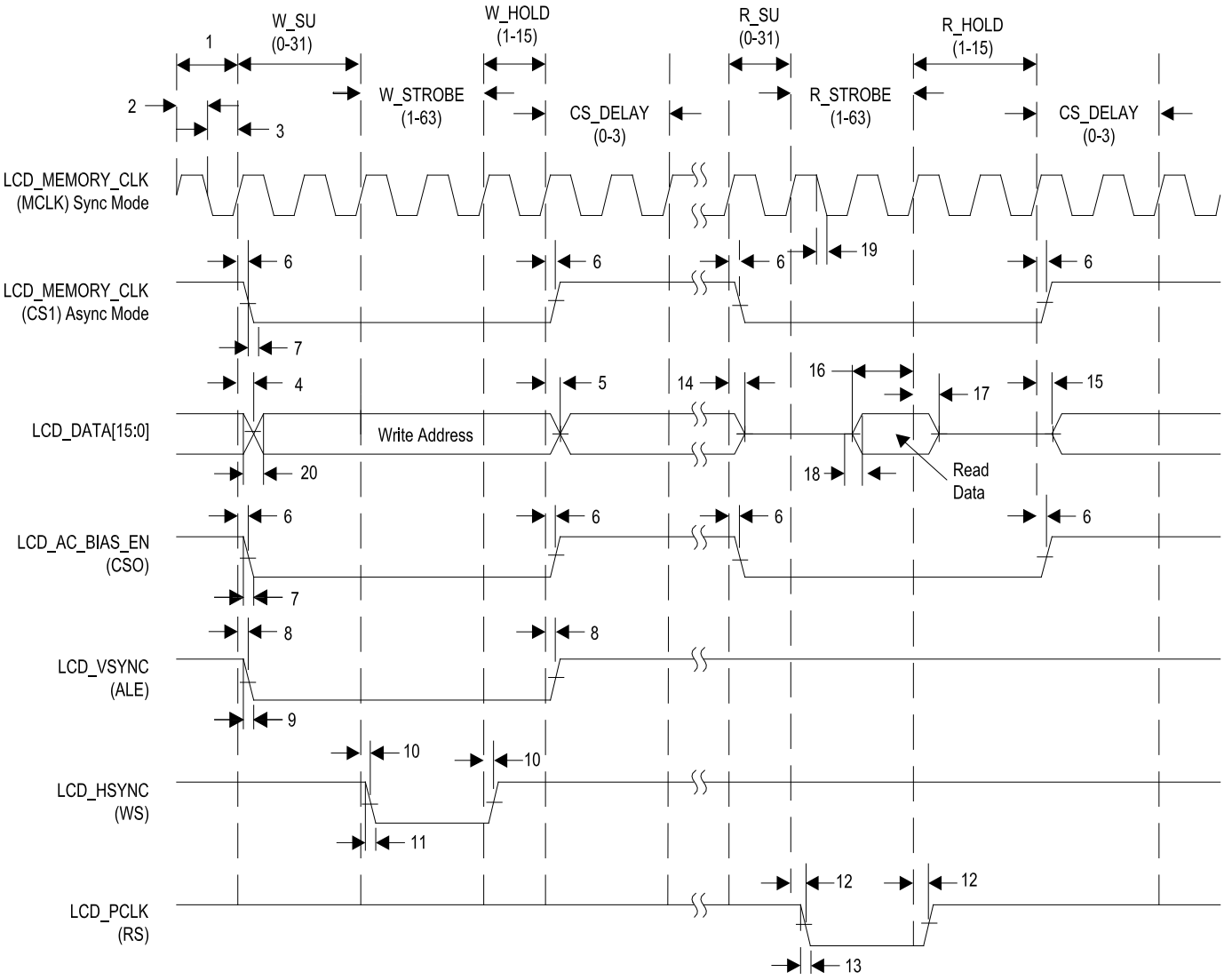
FIGURE 69. Micro-Interface Graphic Display Motorola Status.



Notes:

A. Intel mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

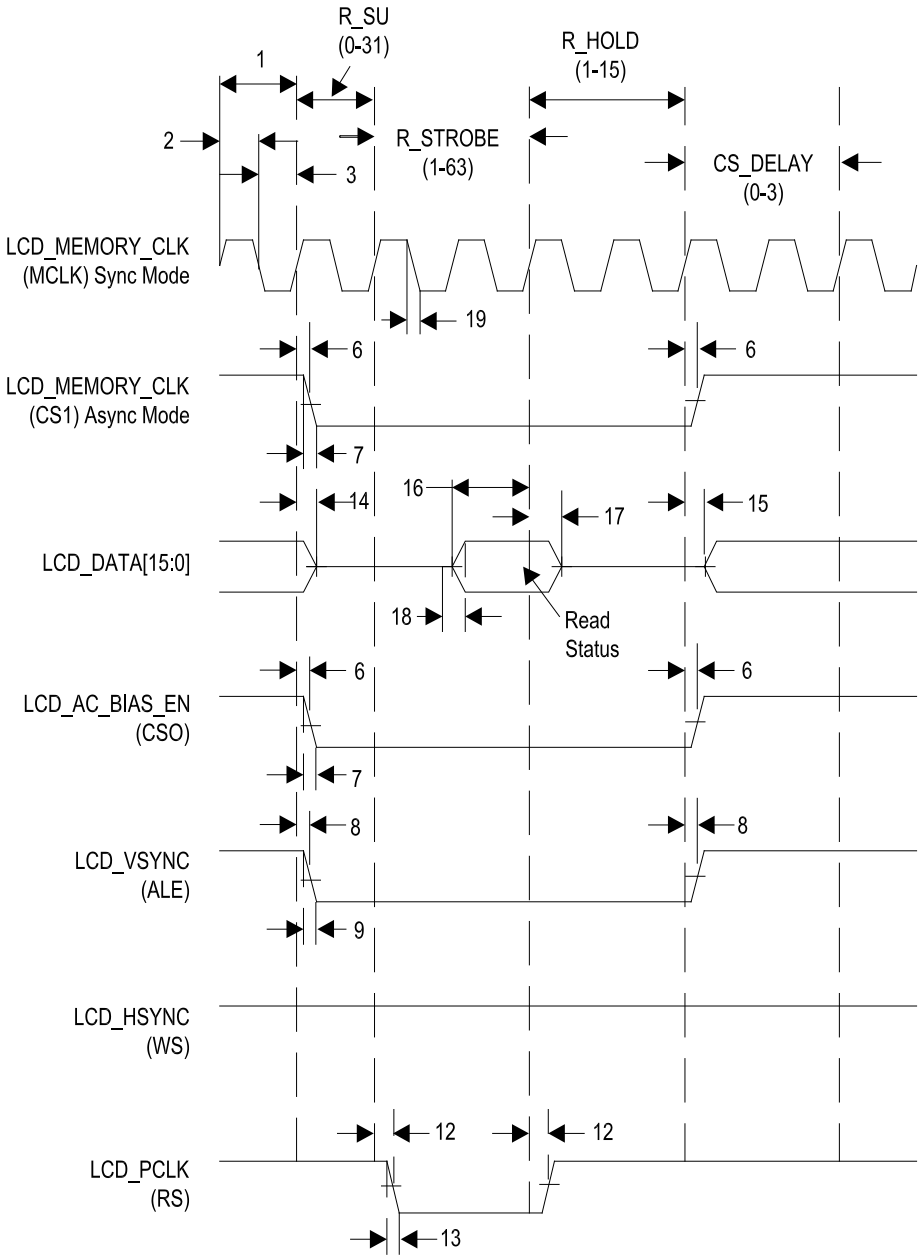
FIGURE 70. Micro-Interface Graphic Display Intel Write.



Notes:

A. Intel mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

FIGURE 71. Micro-Interface Graphic Display Intel Read.



Notes:

A. Intel mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

FIGURE 72. Micro-Interface Graphic Display Intel Status.

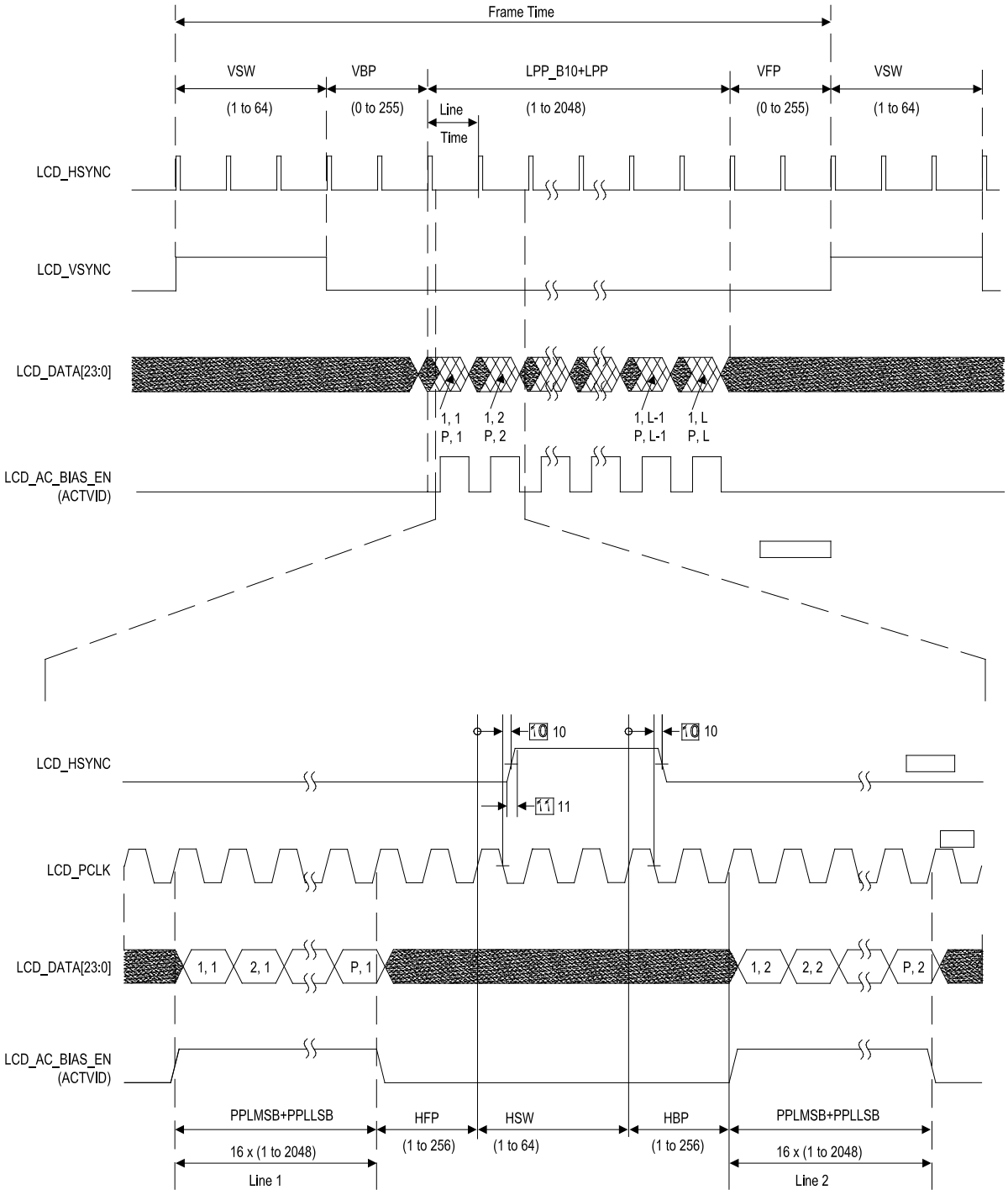
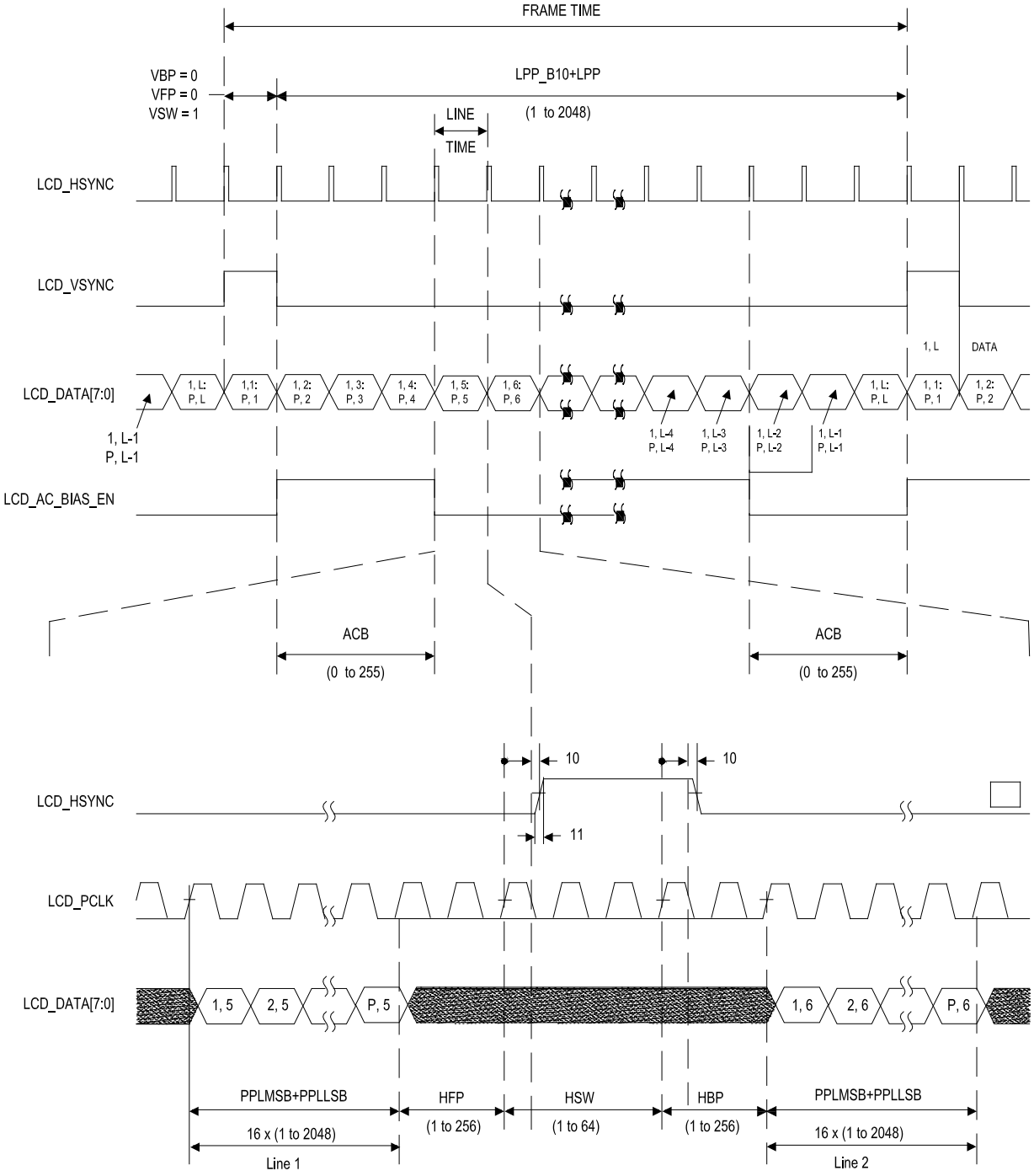


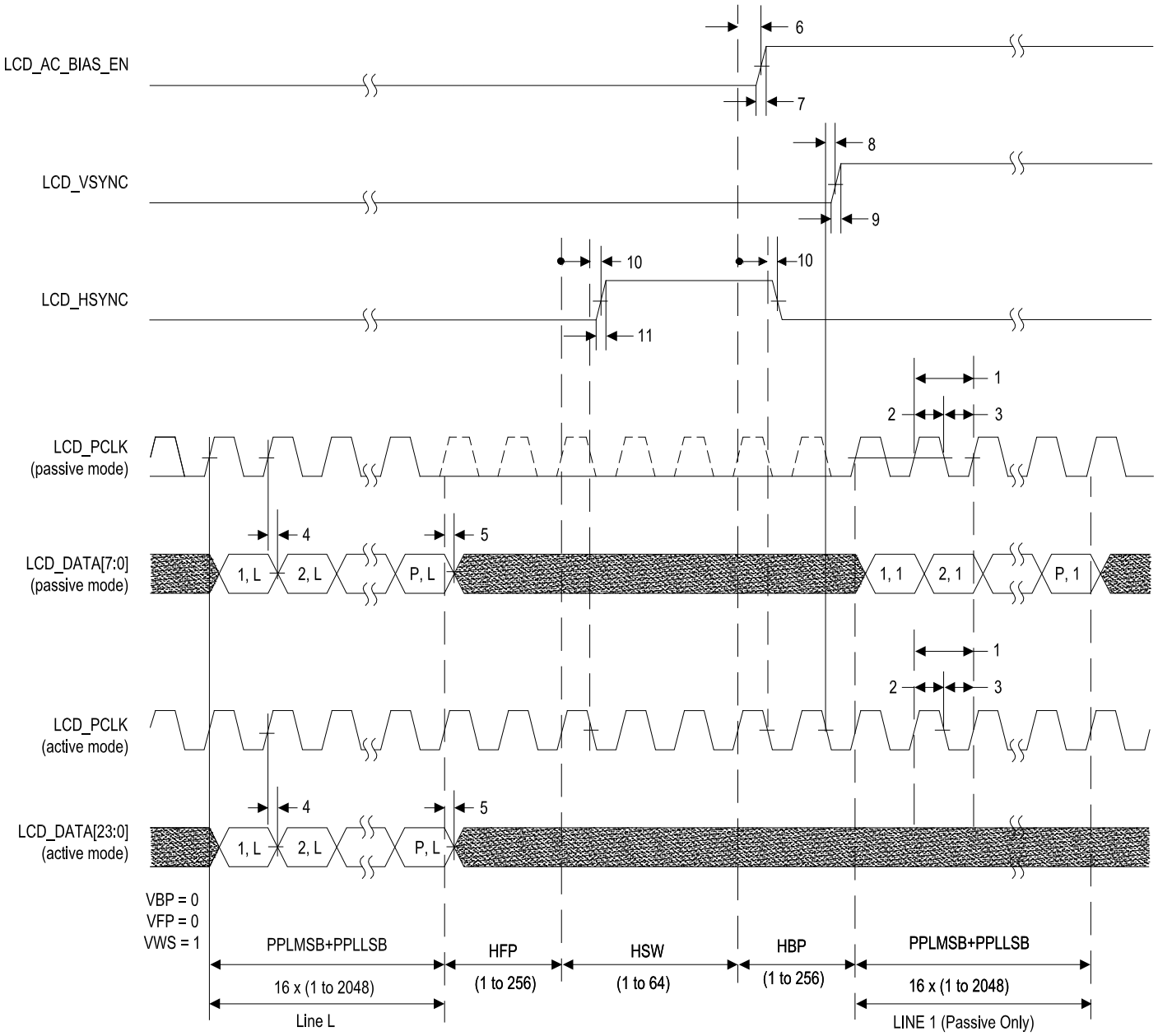
FIGURE 73. LCD Raster-Mode Active.



Notes:

A. The dashed portion of LCD_PCLK is only shown as a reference of the internal clock that sequences the other signals.

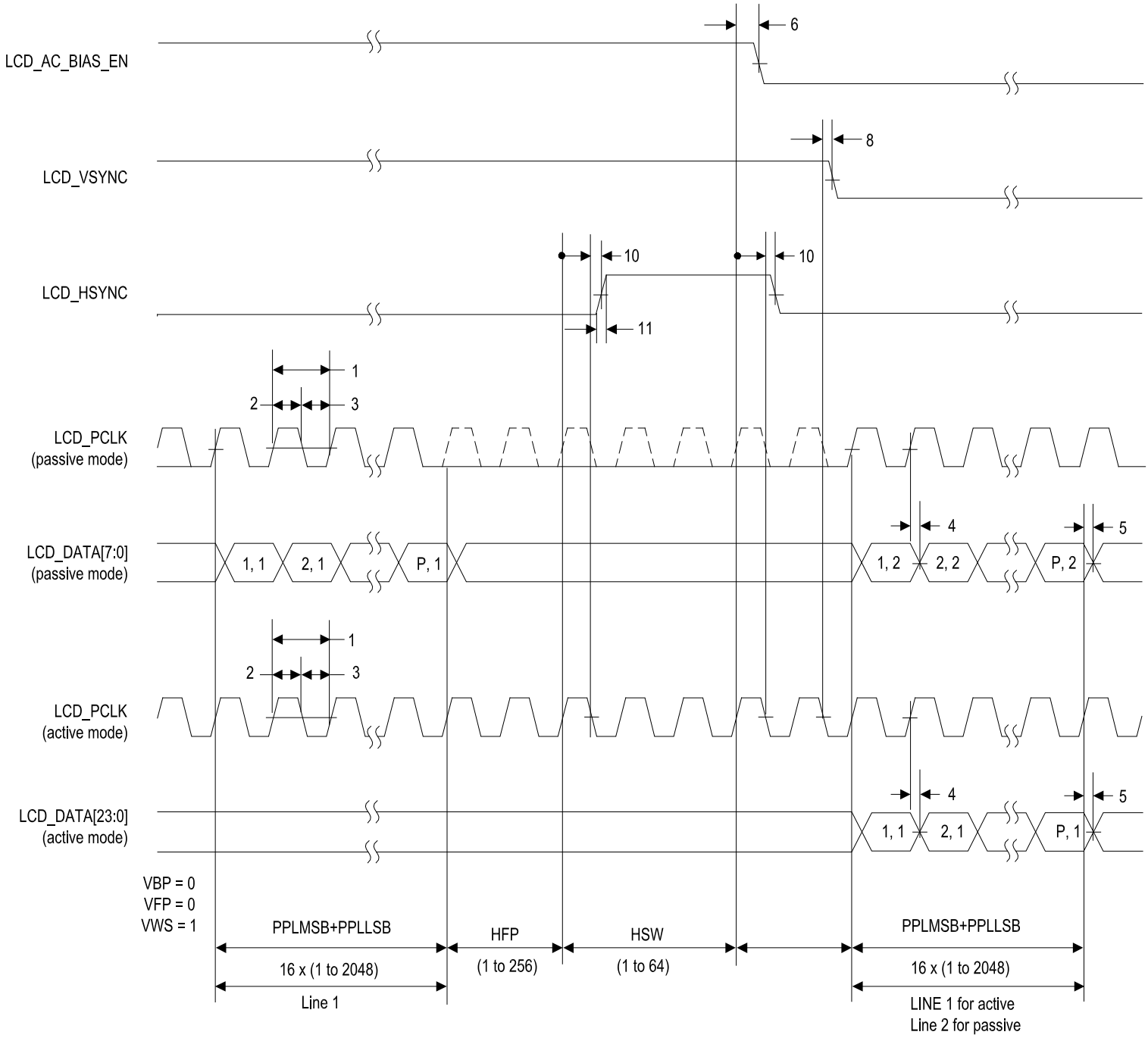
FIGURE 74. LCD Raster-Mode Passive.



Notes:

A. The dashed portion of LCD_PCLK is only shown as a reference of the internal clock that sequences the other signals.

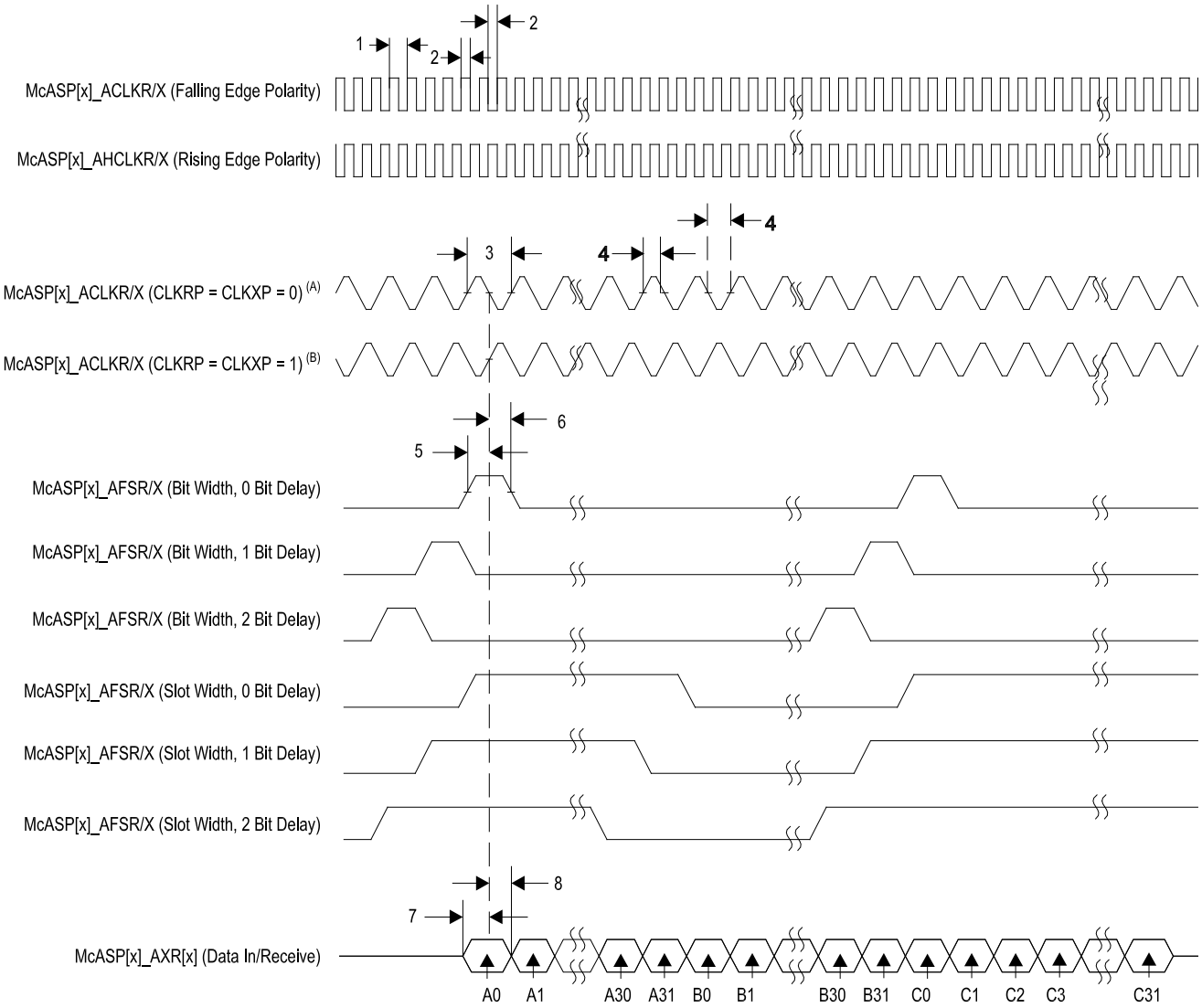
FIGURE 75. LCD Raster-Mode Control Signal Activation.



Notes:

A. The dashed portion of LCD_PCLK is only shown as a reference of the internal clock that sequences the other signals.

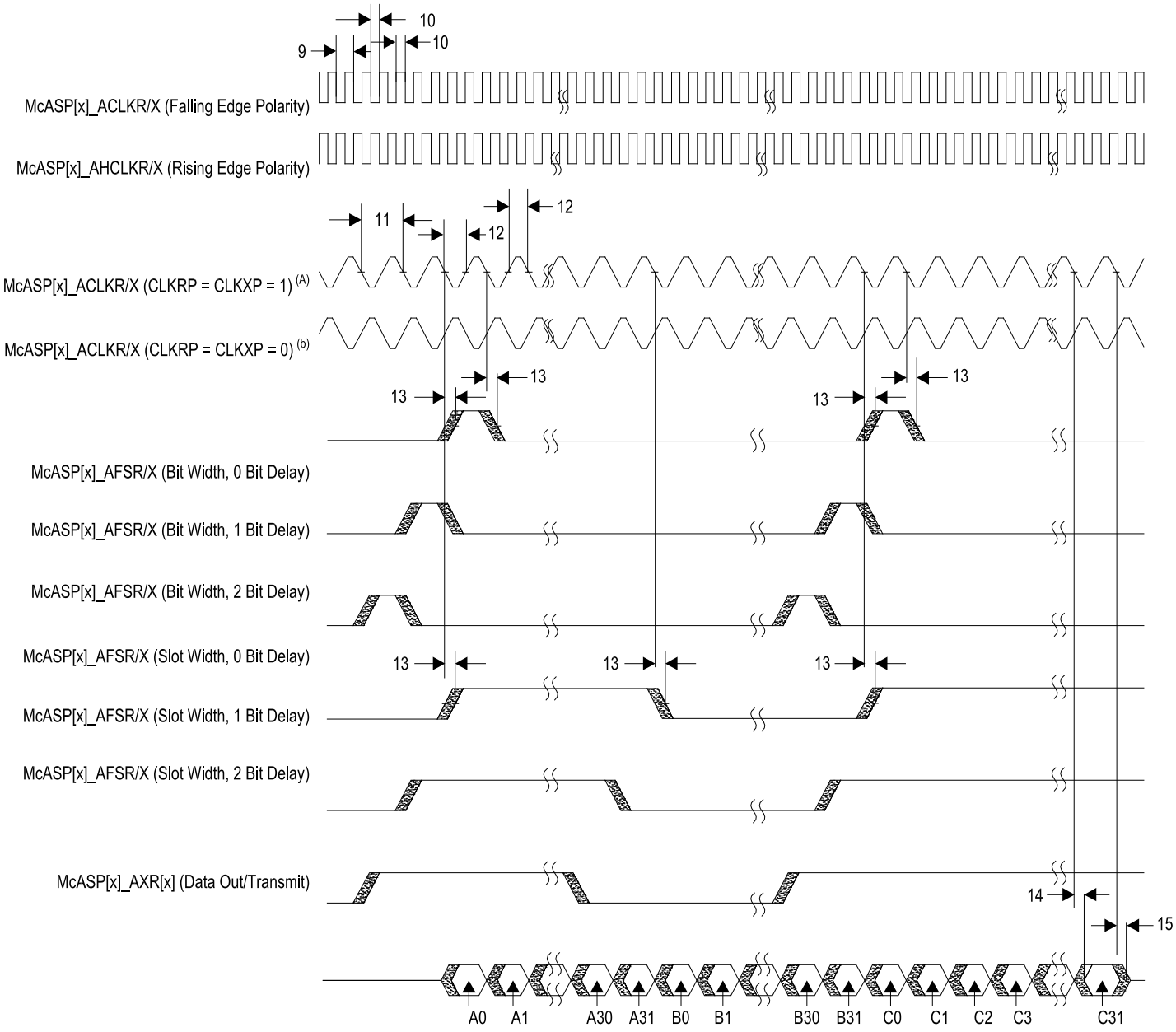
FIGURE 76. LCD Raster-Mode Control Signal Deactivation.



Notes:

A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).
B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

FIGURE 77. McASP Input Timing.



Notes:

A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).
B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

FIGURE 78. McASP Output Timing

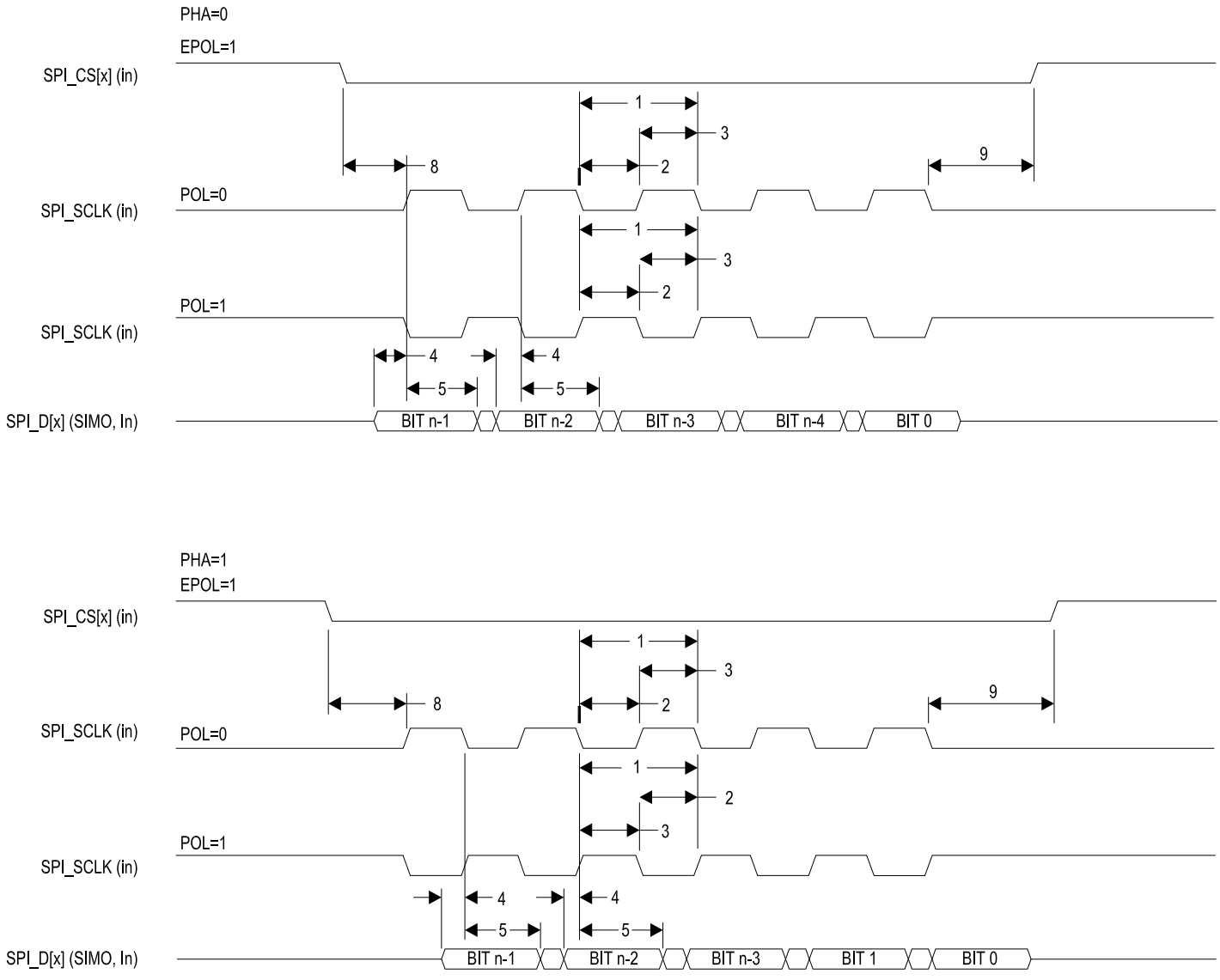


FIGURE 79. SPI Slave Mode Receive Timing.

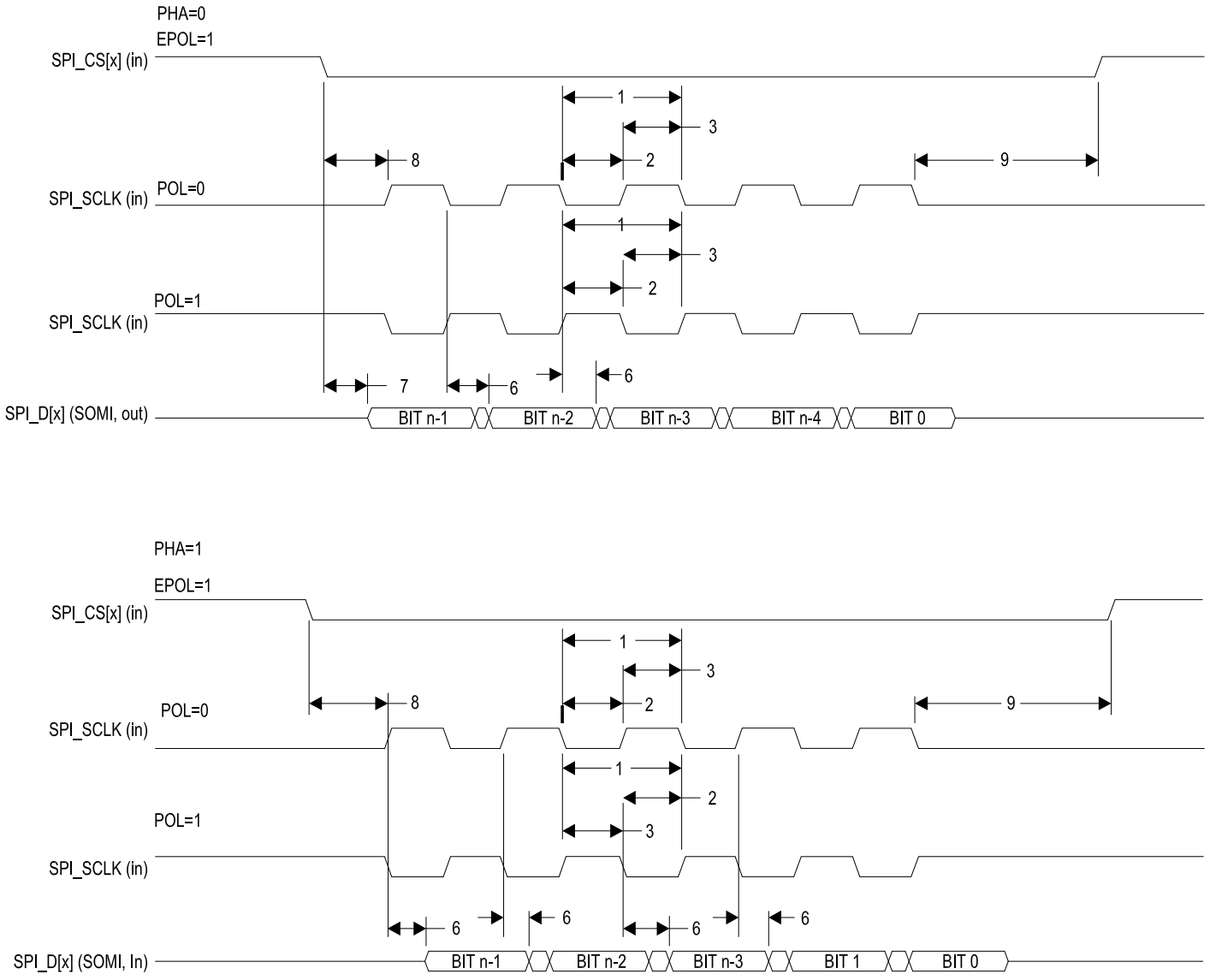


FIGURE 80. SPI Slave Mode Transmit Timing.

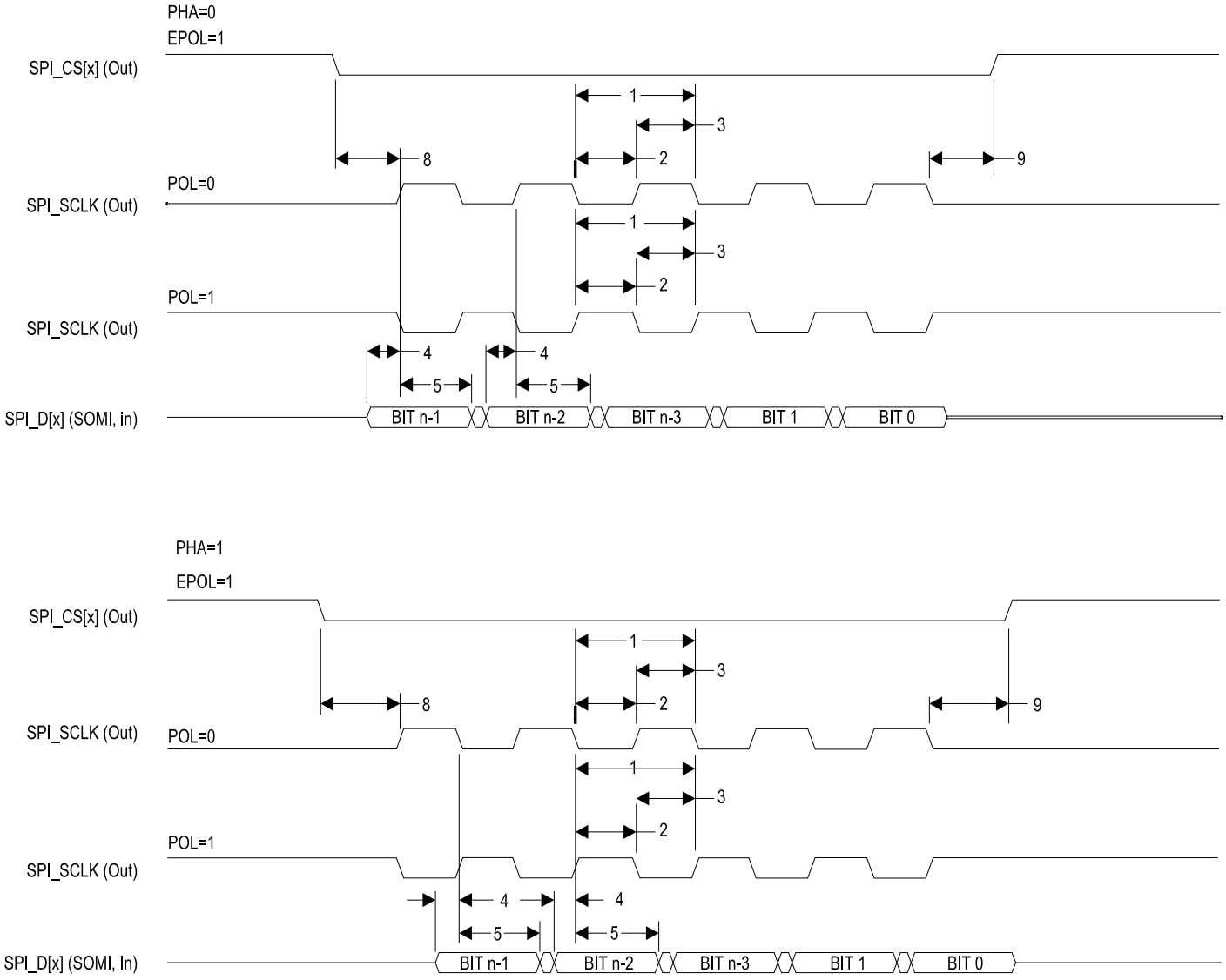


FIGURE 81. SPI Master Mode Receive Timing.

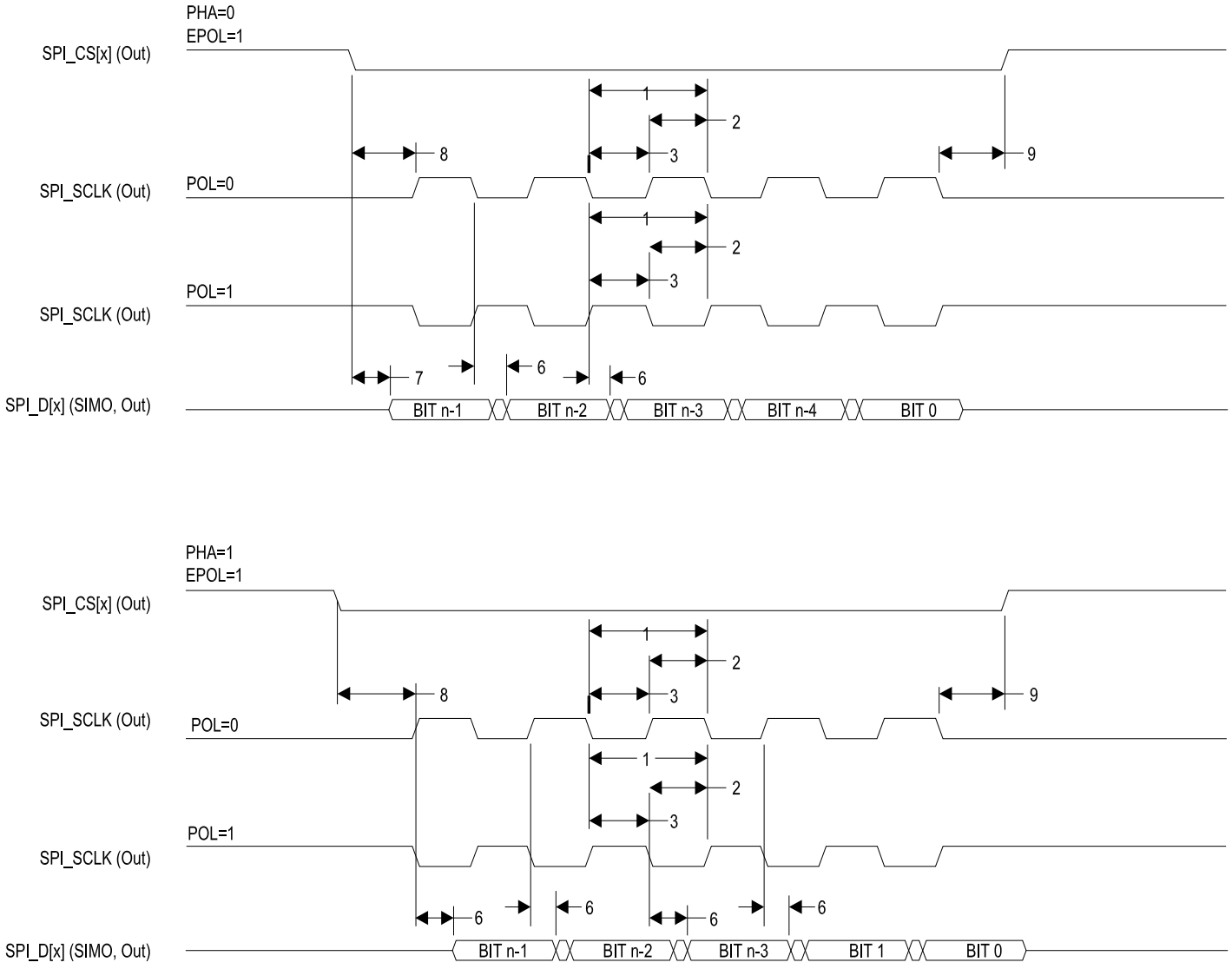


FIGURE 82. SPI Master Mode Transmit Timing.

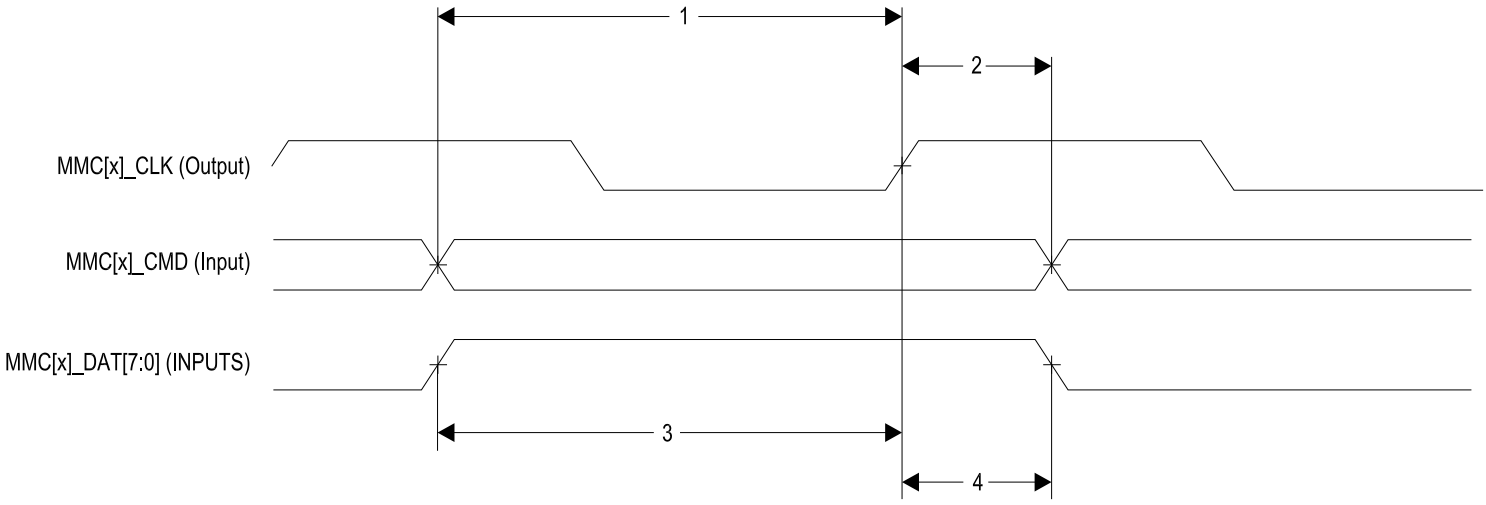


FIGURE 83. MMC[x]_CMD and MMC[x]_DAT[7:0] Input Timing.

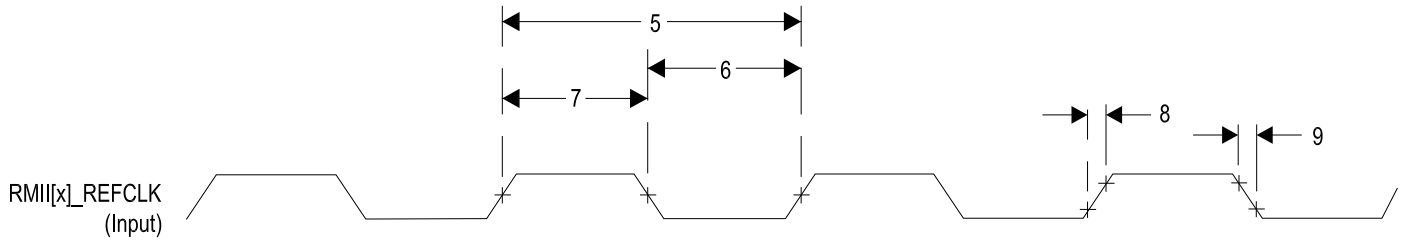


FIGURE 84. MMC[x]_CLK Timing.

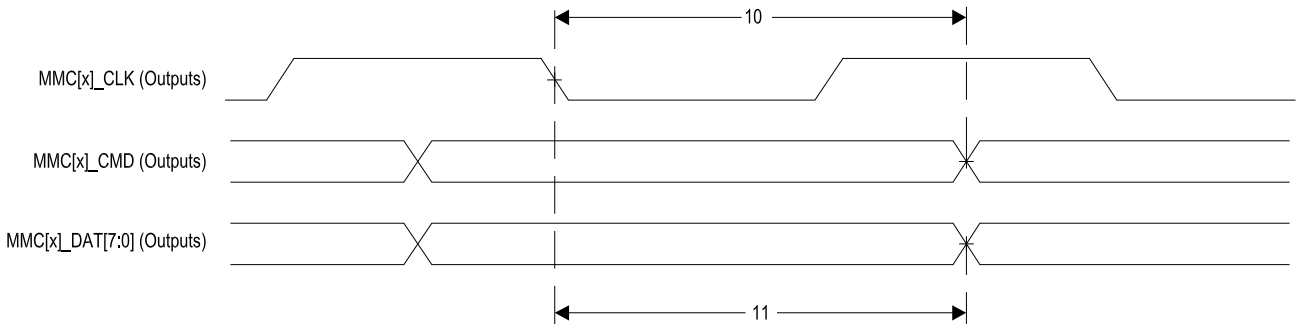


FIGURE 85. MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—Standard Mode.)

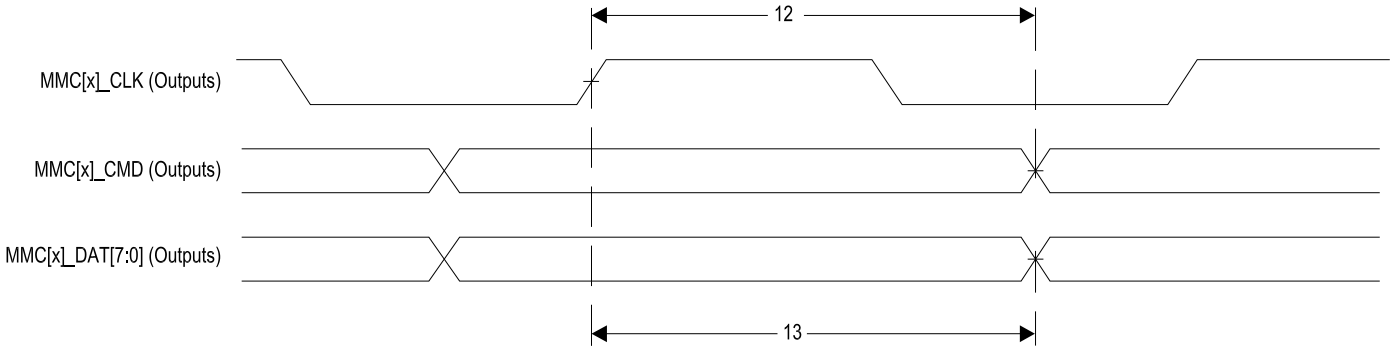


FIGURE 86. MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—High Speed Mode.)

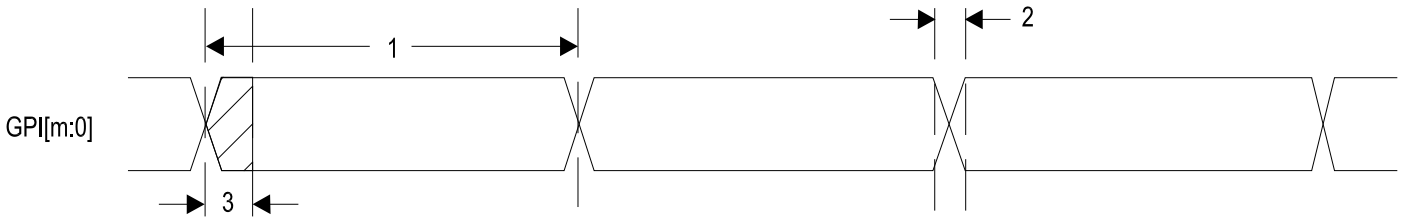


FIGURE 87. PRU-ICSS PRU Direct Input Timing.

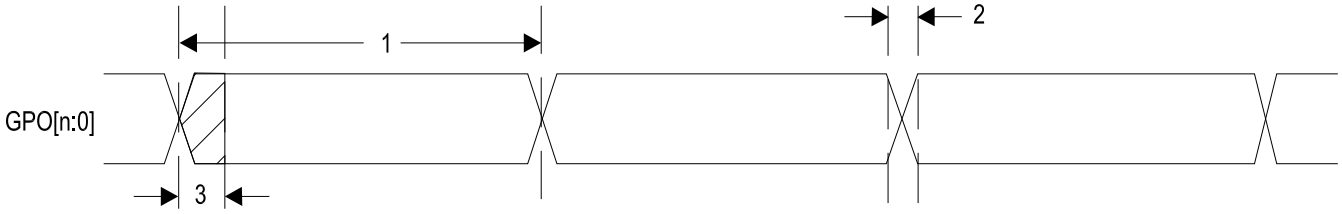


FIGURE 88. PRU-ICSS PRU Direct Output Timing.

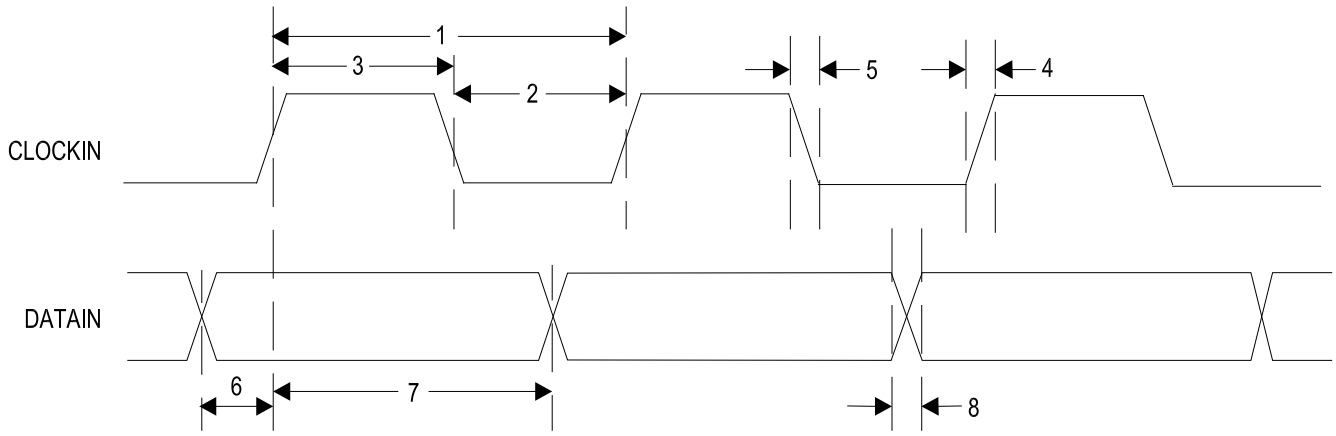


FIGURE 89. PRU-ICSS PRU Parallel Capture Timing - Rising Edge Mode.

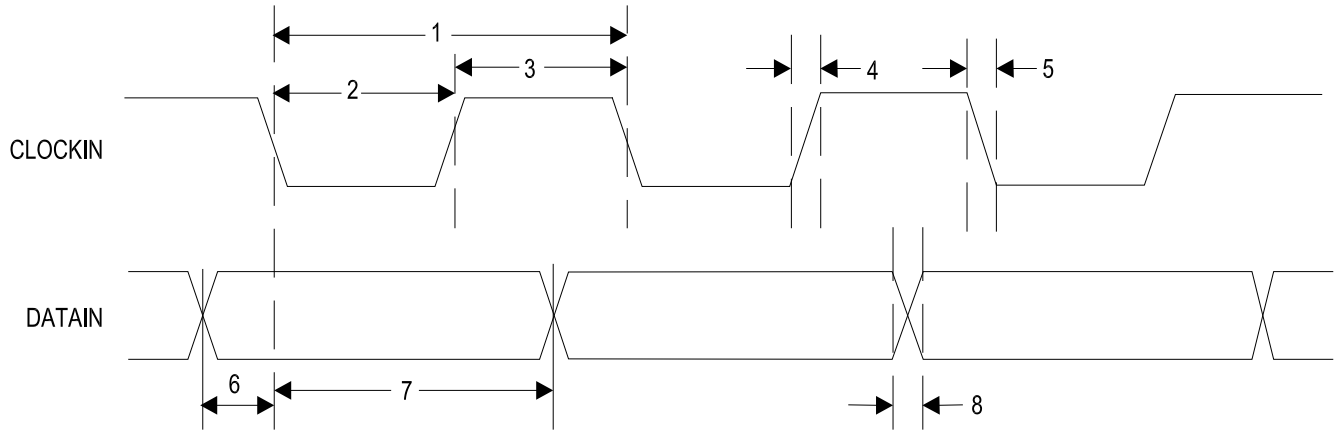


FIGURE 90. PRU-ICSS PRU Parallel Capture Timing - Falling Edge Mode.

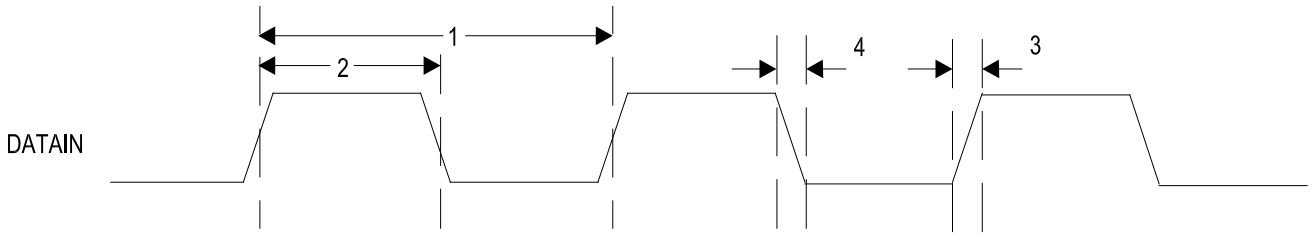


FIGURE 91. PRU-ICSS PRU Shift In Timing.

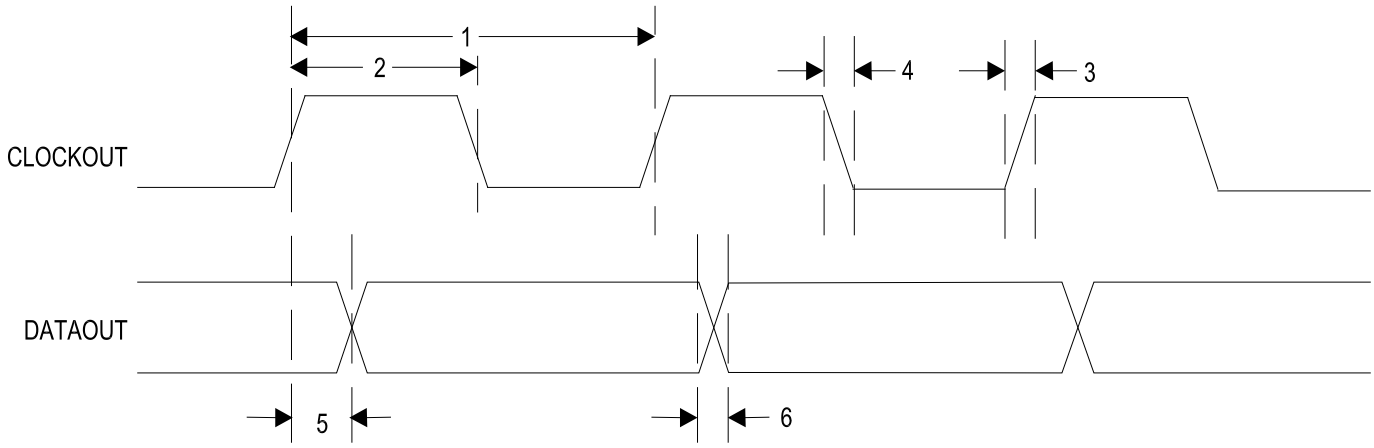


FIGURE 92. PRU-ICSS PRU Shift Out Timing.

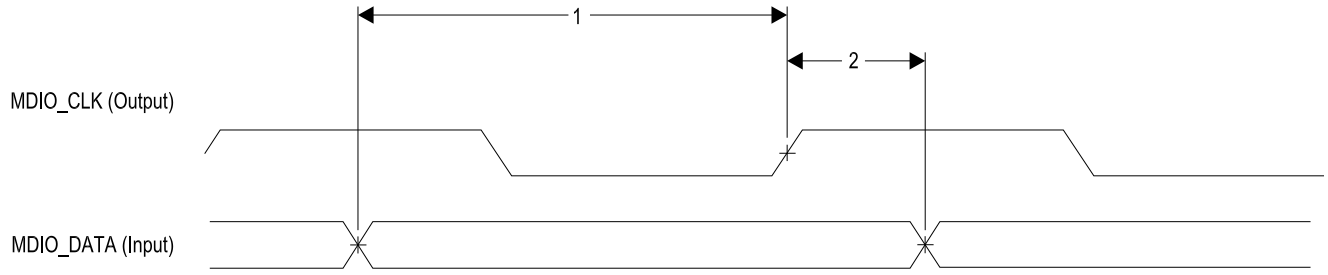


FIGURE 93. PRU-ICSS MDIO_DATA Timing - Input Mode.

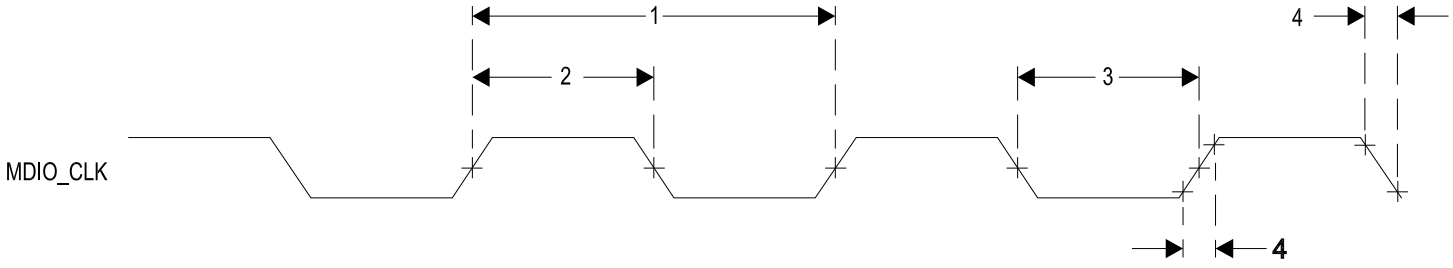


FIGURE 94. PRU-ICSS MDIO_CLK Timing.

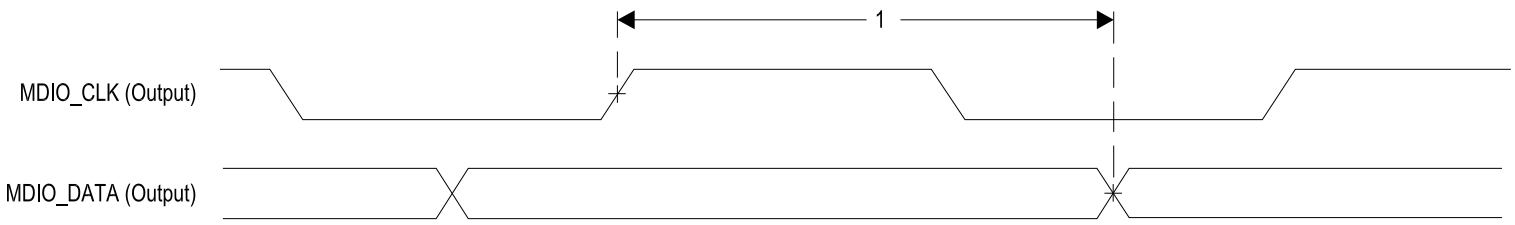


FIGURE 95. PRU-ICSS MDIO_DATA Timing – Output Mode.

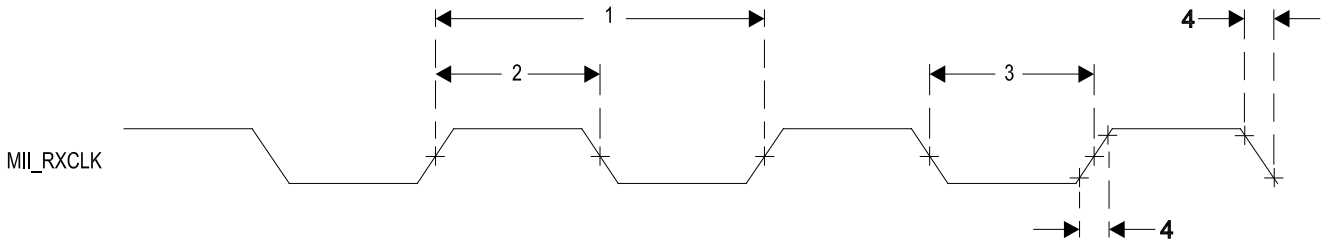


FIGURE 96. PRU-ICSS MII_RXCLK Timing.

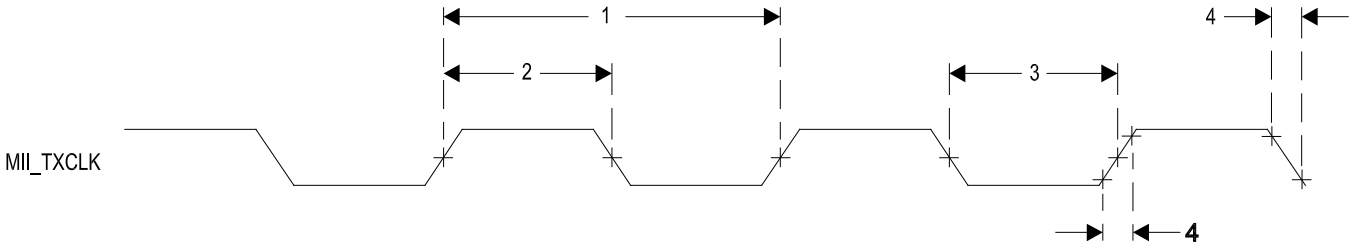


FIGURE 97. PRU-ICSS MII_TXCLK Timing.

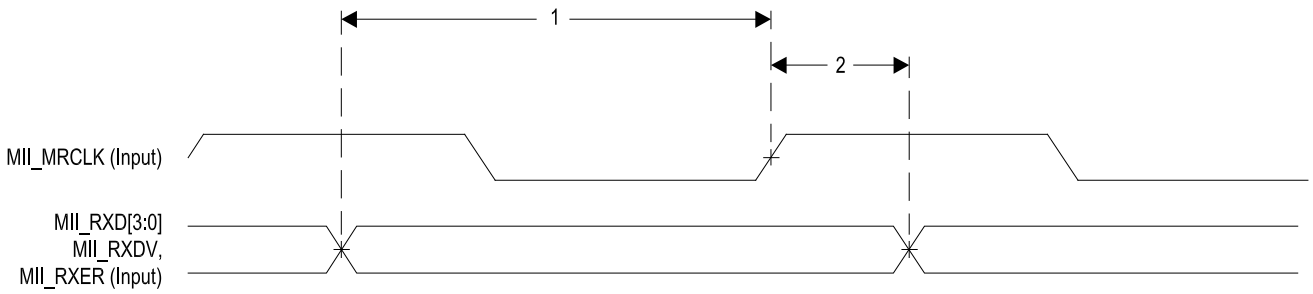


FIGURE 98. PRU-ICSS MII_RXD[3:0], MII_RXDV, and MII_RXER Timing.

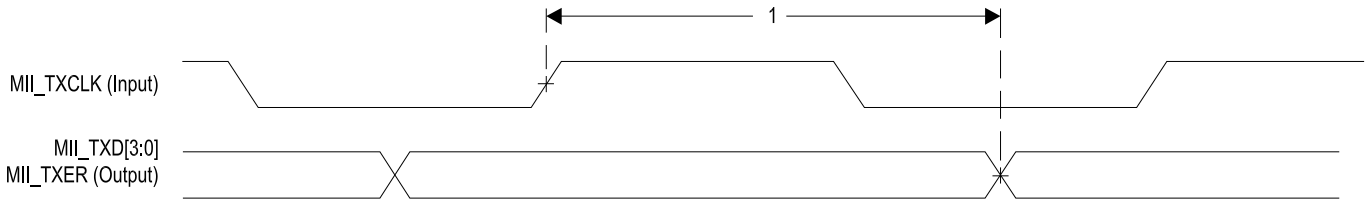


FIGURE 99. PRU-ICSS MII_TXD[3:0], MII_TXEN Timing.)

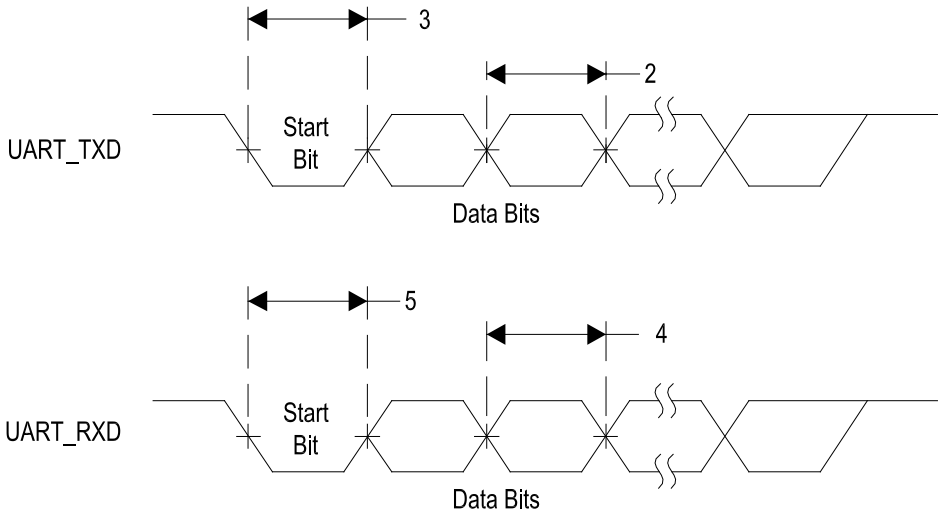


FIGURE 100. PRU-ICSS UART Timing.

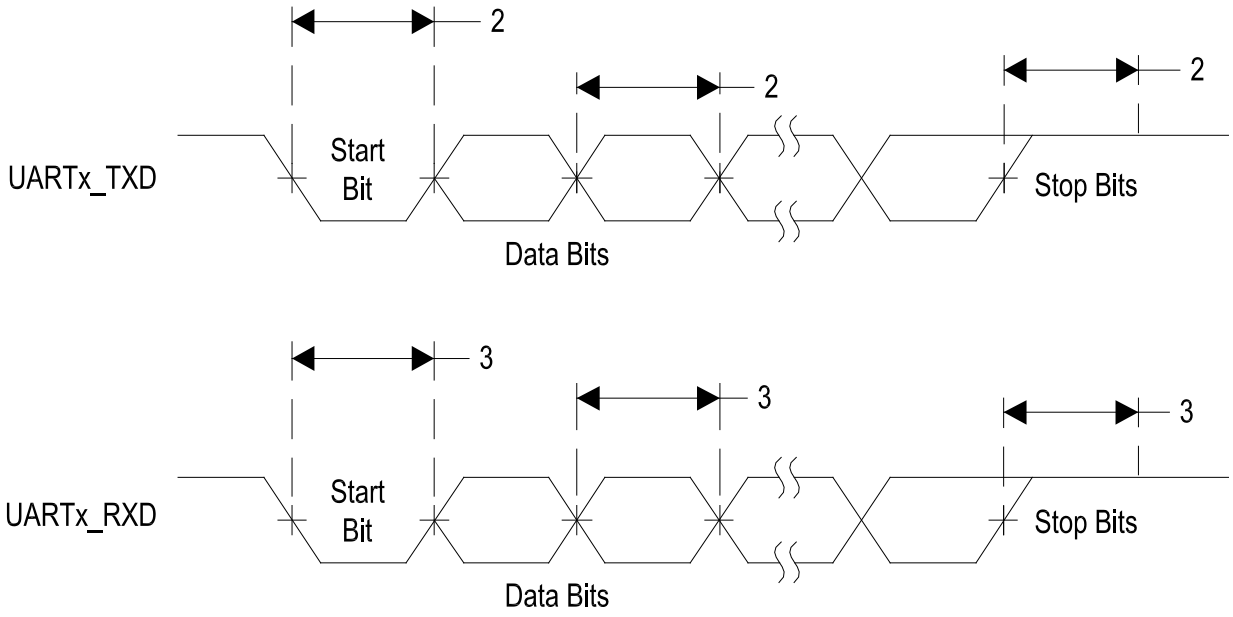


FIGURE 101. UART Timing.

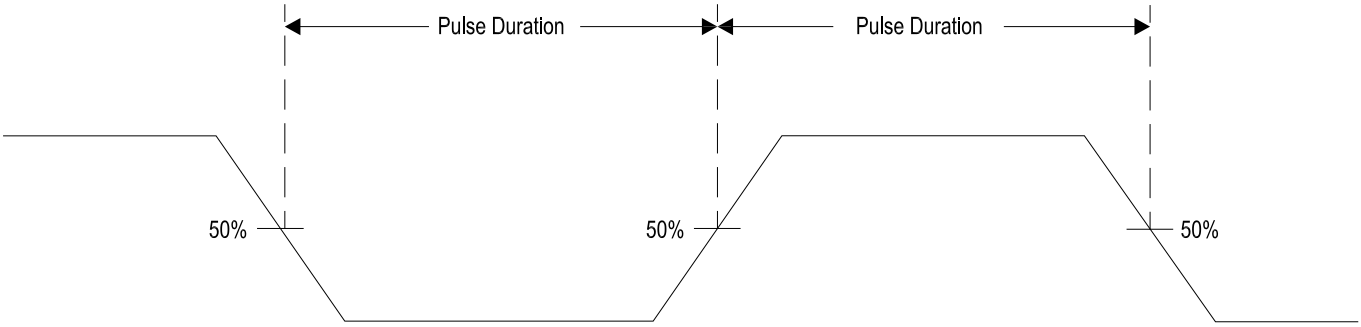


FIGURE 102. UART IrDA Pulse Parameters.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Device Marking
V62/15602-01XF 2/	01295	AM3358BGCZA80EP	M3358BGCZA80EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of Sn = 63%,, Pb = 34.5, Ag = 2% and Sb = 0.5 %.

CAGE code	Source of supply
01295	Texas Instruments, Inc. 12500 TI Blvd. Dallas, TX 75243