REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	17-08-21	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	23-04-20	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12										

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** http://www.landandmaritime.dla.mil/
Original date of drawing YY MM DD 09-11-09	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL CMOS, 3.0 V TO 5.5 V, 12 BIT, 200 KSPS, 4-/8 CHANNEL, LOW POWER SERIAL ANALOG TO DIGITAL CONVERTER WITH AUTOPOWER DOWN, MONOLITHIC SILICON
	SIZE A / **CAGE CODE** 16236	**DWG NO.** V62/10603
	REV B	**PAGE** 1 OF 12

AMSC N/A

5962-V090-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.0 V to 5.5 V, 12 bit, 200 KSPS, 4-/8 channel, low power serial analog to digital converter with auto power down microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/10603	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TLV2548-EP	3.0 V to 5.5 V, 12 bit, 200 KSPS, 4-/8 channel, low power serial analog to digital converter with auto power down

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-153	Plastic Small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (GND to V_{CC}) ..... -0.3 V to 6.5 V
Analog input voltage range, ... -0.3 V to V_{CC} + 0.3 V
Reference input voltage ..... V_{CC} + 0.3 V
Digital input voltage range ..... -0.3 V to V_{CC} + 0.3 V
Operating virtual junction temperature range, T_J ..... -55°C to 150°C
Operating free air temperature range, T_A ..... -55°C to 125°C
Storage temperature range (T_{STG})..... -65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Dissipation ratings:

Package	T_A < 25°C Power rating	Derating factor Above T_A = 25°C 2/	T_A = 125°C power rating
Case outline X	977 mW	7.8 mW/°C	195 mW

1.4 Recommended operating conditions. 3/

Parameter		Symbol	Min	Max	Unit
Supply voltage		V_{CC}	3.0	5.5	V
Analog input voltage 4/			0	V_{CC}	V
High level control input voltage		V_{IH}	2.1		V
Low level control input voltage		V_{IL}		0.6	V
Delay time, delay from $\overline{CS}$ falling edge to FS rising edge (See figure 4)		$t_{d(CSL-FSH)}$	0.5		SCLKs
Delay time, delay from 16th SCLK falling edge to $\overline{CS}$ rising edge (FS = 1), or 17th rising edge (FS is active) (See figure 4 and 7)		$t_{d(SCLK-CSH)}$	0.5		SCLKs
Setup time, FS rising edge before SCLK falling edge (See figure 4)		$t_{su(FSH-SCLKL)}$	20		ns
Hold time, FS hold high after SCLK falling edge (See figure 4)		$t_{h(FSH-SCLKL)}$	30		ns
Pulse width, $\overline{CS}$ high time (See figure 4 and 7)		$t_{wH(CS)}$	100		ns
Pulse width, FS high time (See figure 4)		$t_{wH(FS)}$	0.75		SCLKs
SCLK cycle time (See figure 4 and 7)	V_{CC} = 3.0 V to 3.6 V	$t_{c(SCLK)}$	67	10000	ns
	V_{CC} = 4.5 V to 5.5 V		50	10000	ns

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ This is the inverse of the traditional junction to ambient thermal resistance ($R_{\theta JA}$). Thermal resistance is not production tested and the value given are for informational purposes only.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ When binary output format is used, analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (000000000000). The device is functional with reference down to 1 V. (VREFP – VREFM – 1); however, the electrical specifications are no longer applicable.

1.4 Recommended operating conditions - Continued. 3/

Parameter			Symbol	Min	Max	Unit
Pulse width, SCLK low time	V_{CC} = 4.5 V		$t_{wL(SCLK)}$	22		ns
(See figure 4 and 7)	V_{CC} = 3.0 V			27		
Pulse width, SCLK high time	V_{CC} = 4.5 V		$t_{wH(SCLK)}$	22		
(See figure 4 and 7)	V_{CC} = 3.0 V			27		
Setup time, SDI valid before failing edge of SCLK (FS is active) or the rising edge of SCLK (FS = 1) (See figure 7)			$t_{su(DI-SCLK)}$	25		
Hold time, SDI hold valid after failing edge of SCLK (FS is active) or the rising edge of SCLK (FS = 1) (See figure 7)			$t_{h(DI-SCLK)}$	5		
Delay time, delay from $\overline{CS}$ falling edge to SDO valid (See figure 4 and 7)			$t_{d(CSL-DOV)}$		25	
Delay time, delay from FS falling edge to SDO valid (See figure 4)			$t_{d(FSL-DOV)}$		25	
Delay time, delay from SCLK falling edge (FS is active) or SCLK rising edge (FS = 1) to SDO valid (See figure 4 and 7)	V_{CC} = 5.5 V	SDO = 0 pF	$t_{d(SCLK-DOV)}$	0.5 SCLK + 5 TYP		
		SDO = 60 pF			0.5 SCLK + 24	
For a date code later than xxx, see the data code from manufacturer data.	V_{CC} = 3.0 V	SDO = 0 pF		0.5 SCLK + 12 TYP		
		SDO = 60 pF			0.5 SCLK + 33	
Delay time, delay from 17th SCLK rising edge (FS is active), or the 16th falling edge (FS = 1) to EOC falling edge (See figure 4 and 7)			$t_{d(SCLK-EOCL)}$	45 TYP		
Delay time, delay from 16th SCLK falling edge to $\overline{INT}$ falling edge (FS = 1), or from the 17th rising edge SCLK to $\overline{INT}$ rising edge. (See figure 4, 5, 6, and 7)			$t_{d(SCLK-INTL)}$	Min $t_{(conv)}$		
Delay time, delay from $\overline{CS}$ falling edge or FS rising edge to $\overline{INT}$ rising edge (See figure 4, 5, 6, and 7)			$t_{d(CLK-INTH)}$ or $t_{d(FSH-INTH)}$		50	
Delay time, delay from $\overline{CS}$ rising edge to $\overline{CSTART}$ falling edge (See figure 5 and 6)			$t_{d(CSH-CSTARTL)}$	100		
Delay time, delay from $\overline{CSTART}$ rising edge to EOC falling edge (See figure 5 and 6)			$t_{d(CSTARTH-EOCL)}$		50	ns
Pulse width, $\overline{CSTART}$ low time (See figure 5 and 6)			$t_{wL(CSTART)}$	Min $t_{(sample)}$		µs
Delay time, delay from $\overline{CSTART}$ rising edge to $\overline{CSTART}$ falling edge (See figure 6)			$t_{d(CSTARTH-CSTARTL)}$	Min $t_{(conv)}$		µs
Delay time, delay from $\overline{CSTART}$ rising edge to $\overline{INT}$ falling edge (See figure 6 and 7)			$t_{d(CSTARTH-INTL)}$	Max $t_{(conv)}$ TYP		µs
Operation free air temperature			T_A	-55	125	ºC

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4 - 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/		Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 5.5 V, I_{OH} = -0.2 mA at 30 pF load		2.4		V
		V_{CC} = 3.0 V, I_{OH} = -20 µA at 30 pF load		V_{CC} – 0.2		
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 0.8 mA at 30 pF load			0.4	
		V_{CC} = 3.0 V, I_{OL} = 20 µA at 30 pF load			0.1	
Off state output current (high-impedance state)	I_{OZ}	V_O = V_{CC}	$\overline{CS}$ = V_{CC}		2.5	µA
		V_O = 0	$\overline{CS}$ = V_{CC}	-2.5		
High level input current	I_{IH}	V_I = V_{CC}			2.5	
Low level input current	I_{IL}	V_I = 0 V			2.5	
Operating supply current, normal short sampling	I_{CC}	$\overline{CS}$ at 0 V, Ext ref	V_{CC} = 4.5 V to 5.5 V		2	mA
			V_{CC} = 3.0 V to 3.3 V		1	
		$\overline{CS}$ at 0 V, Int ref	V_{CC} = 4.5 V to 5.5 V		2.4	
			V_{CC} = 3.0 V to 3.3 V		1.7	
Operating supply current, extended sampling		$\overline{CS}$ at 0 V, Ext ref	V_{CC} = 4.5 V to 5.5 V	1.1	TYP	
			V_{CC} = 3.0 V to 3.3 V	1	TYP	
		$\overline{CS}$ at 0 V, Int ref	V_{CC} = 4.5 V to 5.5 V	2.1	TYP	
			V_{CC} = 3.0 V to 3.3 V	1.6	TYP	
Power down supply current for all digital input, 0 ≤ V_I ≤ 0.3 V or V_I ≥ V_{CC} – 0.3 V, SCLK = 0	$I_{CC(PD)}$	V_{CC} = 4.5 V to 5.5 V, Ext clock		1	TYP	µA
		V_{CC} = 3.0 V to 3.3 V, Ext clock		1	TYP	
Auto power down current for all digital input, 0 ≤ V_I ≤ 0.3 V or V_I ≥ V_{CC} – 0.3 V, SCLK = 0	$I_{CC(AUTOPWDN)}$	V_{CC} = 4.5 V to 5.5 V, Ext clock, Ext ref		1.0 3/	TYP	
		V_{CC} = 3.0 V to 3.3 V, Ext clock, Ext ref		1.0 4/	TYP	
Selected channel leakage current		Selected channel at V_{CC}			2.5	
		Selected channel at 0 V			2.5	
Maximum static analog reference current into REFP (use external reference)		VREFP = V_{CC} = 5.5 V, VREFM = GND		1	TYP	
Input capacitance	C_i	Analog inputs			50	pF
		Control inputs			25	
Input MUX ON resistance	Z_i	V_{CC} = 4.5 V			500	Ω
		V_{CC} = 2.7 V			600	
AC specifications						
Signal to noise ratio + distortion	SINAD	f_I = 12 kHz at 200 KSPS		65		dB
Total harmonic distortion	THD	f_I = 12 kHz at 200 KSPS	T_A = -55ºC		-73	
			All other temperature		-75	
Effective number of bits	ENOB	f_I = 12 kHz at 200 KSPS		11.6	TYP	Bits
Spurious free dynamic range	SFDR	f_I = 12 kHz at 200 KSPS			-75	dB
Analog input						
Full power bandwidth, -3 dB				1 TYP		MHz
Full power bandwidth, -1 dB				500 TYP		kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Conditions 2/		Limits Min	Limits Max	Unit
Reference specifications 5/ (0.1 µF and 10 µF between REFP and REFM pins)							
Positive reference input voltage		REFP	V_{CC} = 3.0 V to 3.3 V		2	V_{CC}	V
Negative reference input voltage		REFM	V_{CC} = 3.0 V to 3.3 V		0	2	
Reference input impedance			V_{CC} = 5.5 V	$\overline{CS}$ = 1, SCLK = 0, (off)	100		MΩ
				$\overline{CS}$ = 0, SCLK = 20 MHz, (on)	20		kΩ
			V_{CC} = 3 V	$\overline{CS}$ = 1, SCLK = 0, (off)	100		MΩ
				$\overline{CS}$ = 0, SCLK = 15 MHz, (on)	20		kΩ
Reference input voltage difference		REFP - REFM	V_{CC} = 3.0 V to 5.5 V		2	V_{CC}	V
Internal reference voltage		REFP - REFM	V_{CC} = 5.5 V	VREF SELECT = 4 V	3.85	4.15	V
			V_{CC} = 5.5 V	VREF SELECT = 2 V	1.925	2.075	
			V_{CC} = 3.0 V	VREF SELECT = 2 V	1.925	2.075	
Internal reference start up time			V_{CC} = 5.5 V, 3 V with 10 µF compensation cap		20 TYP		ms
Internal reference temperature coefficient					2.075	40 5/	PPM/ ºC
Operating characteristics							
Integral linearity error (INL) 6/		EL				±1.2	LSB
Differential linearity error (DNL)		ED	7/			±1.2	
Offset error 8/		EO	7/	T_A = 25ºC and 125ºC	-4	6	
				T_A = -55ºC	-4	6.2	
Full scale error 8/		EFS	7/	T_A = 25ºC and 125ºC	-4	6	
				T_A = -55ºC	-4	7.6	
Self test output code 9/			SDI = B000h		800 h (2048D)		
			SDI = C000h		000h (0D)		
			SDI = D000h		FFFh (4095D)		
Conversion time	Internal OSC	$t_{(conv)}$				4.65	µs
	External SCLK				(14 x DIV)	/ f_{SCLK}	
Sampling time		$t_{(sample)}$	With a maximum of 1 kW input source impedance		600		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over operating free air temperature range, V_{CC} = V_{REFP} = 3 V to 5.5 V, V_{REFM} = 0 V, SCLK frequency = 20 MHz at 5 V, 15 MHz at 3 V (unless otherwise noted). All typical values are at V_{CC} = 5 V, T_A = 25ºC

3/ 1.2 mA if internal reference is used, 165 µA if internal clock is used.

4/ 0.8 mA if internal reference is used, 116 µA if internal clock is used.

5/ Specified by design.

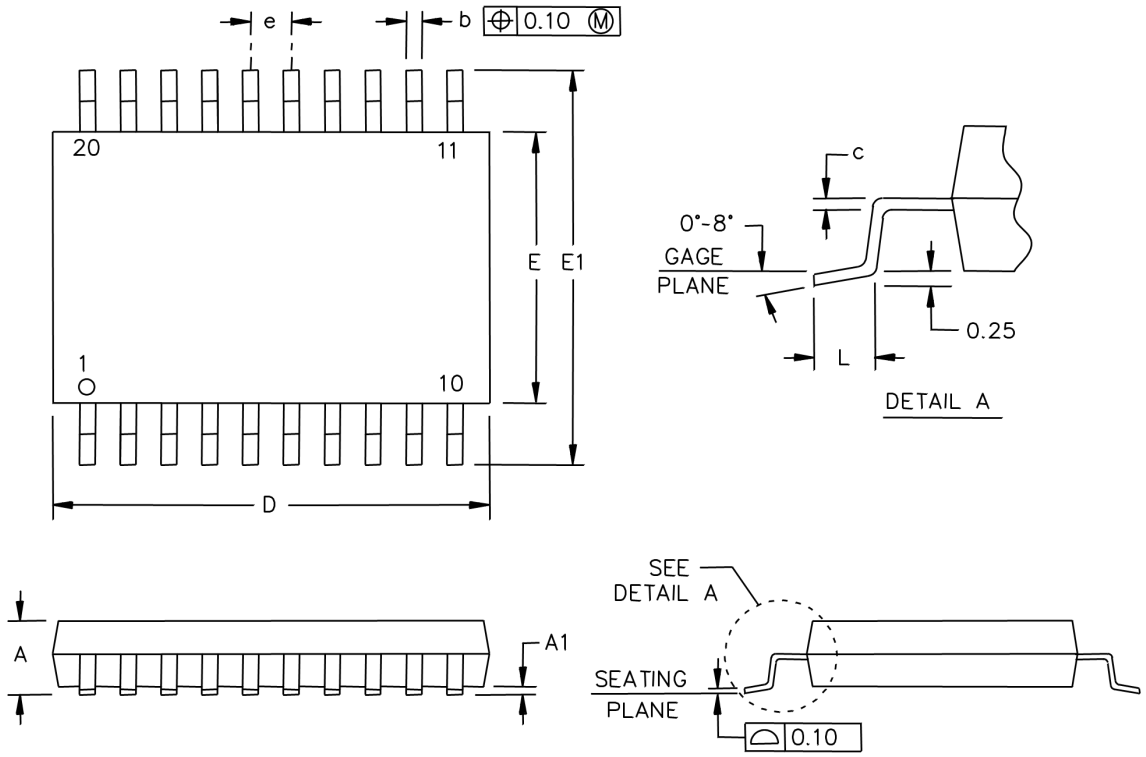
6/ Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.

7/ Analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (000000000000).

8/ Zero error is the difference between 000000000000 and the converted output for zero input voltage: full scale error is the difference between 111111111111 and the converted output for full scale input voltage.

9/ Both the input data and the output codes are expressed in positive logic.

Case X



Dimensions

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.15	NOM	L	0.50	0.75
D	6.40	6.60			

NOTES:
1. All linear dimensions are in millimeters..
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

Case outlines X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	SDO	11	A5
2	SDI	12	A6
3	SCLK	13	A7
4	EOC($\overline{\text{INT}}$)	14	$\overline{\text{CSTART}}$
5	V_{CC}	15	GND
6	A0	16	$\overline{\text{PWDN}}$
7	A1	17	FS
8	A2	18	REFM
9	A3	19	REFP
10	A4	20	$\overline{\text{CS}}$

FIGURE 2. Terminal connections.

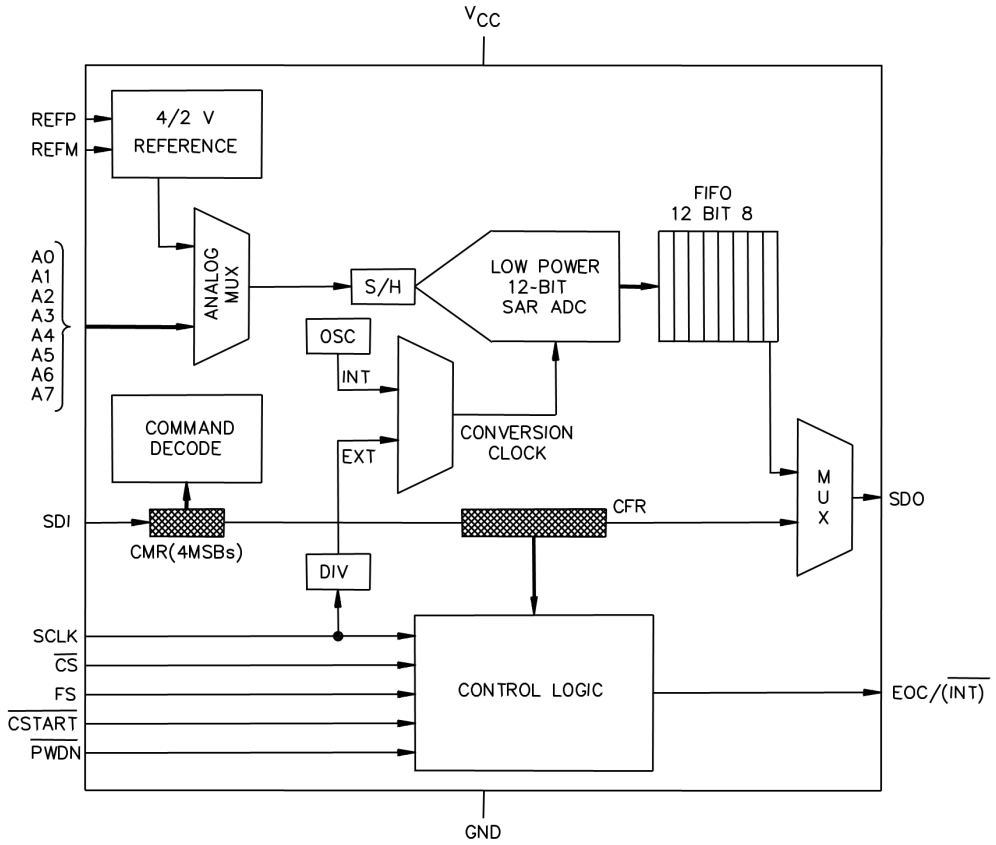
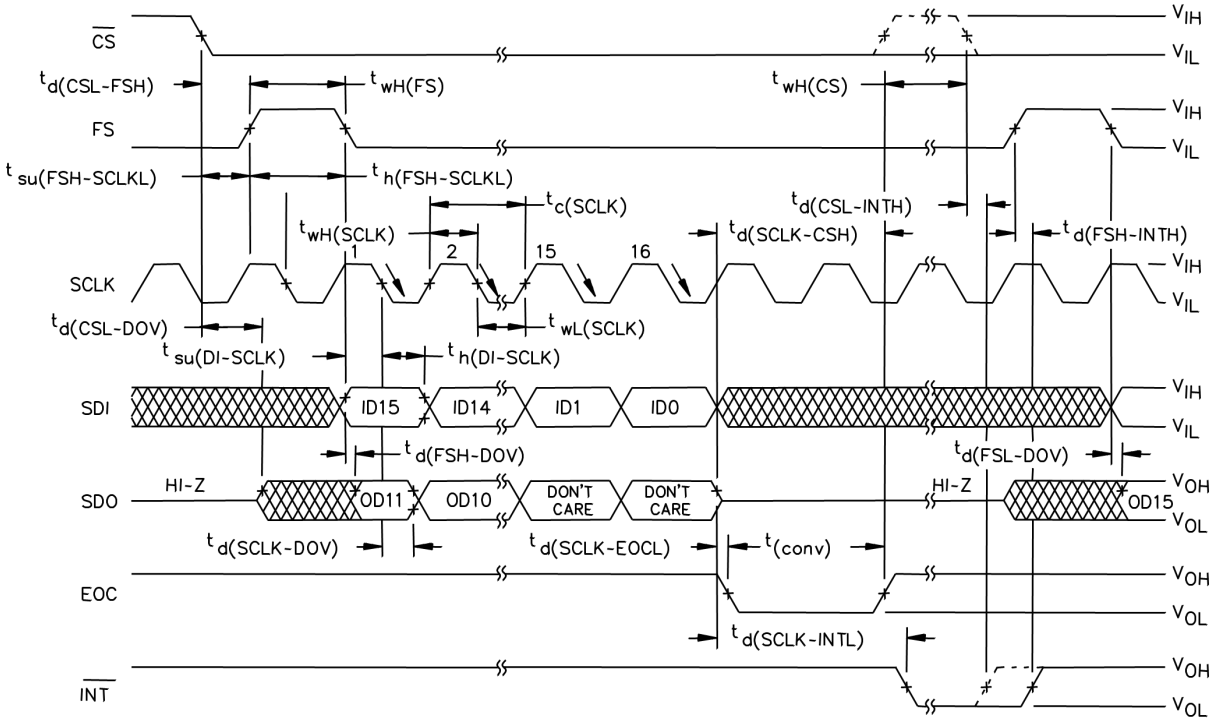
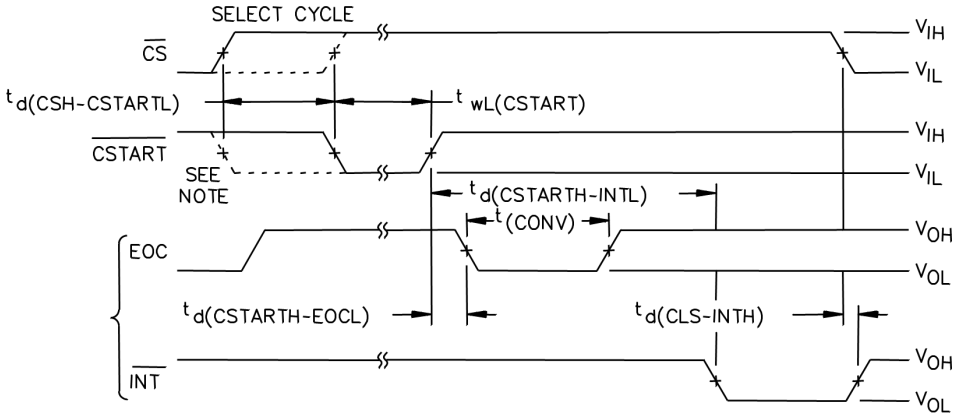


FIGURE 3. Functional block diagram.



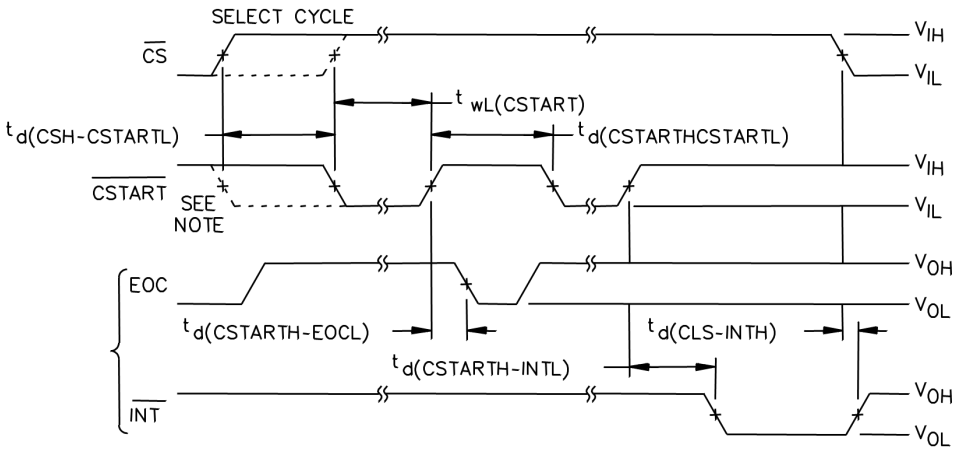
CRITICAL TIMING, DSP MODE(NORMAL SAMPLING, FS IS ACTIVE)

FIGURE 4. Timing waveforms.



CRITICAL TIMING (EXTENDED SAMPLING, SINGLE SHOT)

FIGURE 5. Timing waveforms.

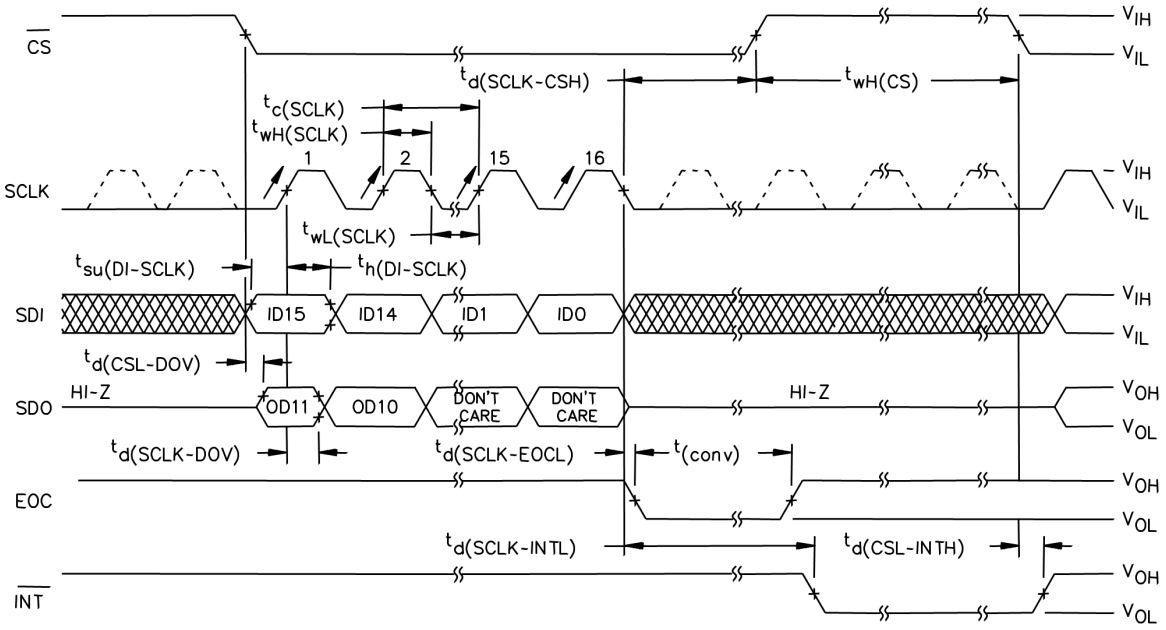


CRITICAL TIMING (EXTENDED SAMPLING, REPEAT/SWEEP/REPEAT SWEEP)

NOTES:

1. $\overline{\text{CSTART}}$ falling edge may come before the riding edge of $\overline{\text{CS}}$ but no sooner than the fifth SCLK of the SELECT CYCLE. In this case, the actual sampling time is measured from the rising edge $\overline{\text{CS}}$ to the rising edge of $\overline{\text{CSTART}}$.

FIGURE 6. Timing waveforms.



CRITICAL TIMING, MICROPROCESSOR MODE(NORMAL SAMPLING, FS=1)

FIGURE 7. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/10603-01XE	01295	TLV2548MPWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243