REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Figure 1, case outline X, corrected the “e” dimension. Updated drawing to remove class M requirements. - drw	12-07-25	Charles F. Saffle
B	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	18-08-24	Charles F. Saffle
C	Figure 2, case outline X, made corrections to terminal numbers 10, 60, and 61. -rrp	19-05-20	Charles F. Saffle

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raj Pithadia

APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
11-07-01

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL-LINEAR, 12 BIT, 1 GSPS, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

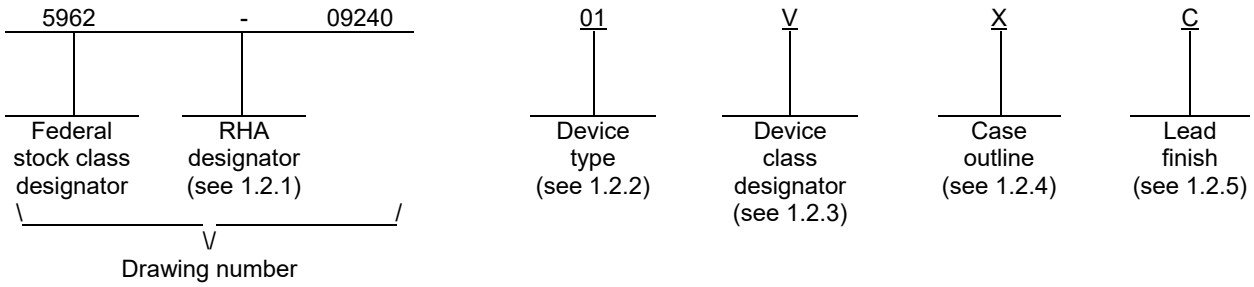
SIZE	CAGE CODE	
A	**67268**	**5962-09240**

SHEET 1 OF 24

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	ADS5400-SP	12 bit, 1 GSPS, analog to digital converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	100	Ceramic nonconductive tie-bar package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/, 2/

Supply voltage:	
5 V analog supply voltage (AVDD5) to ground (GND)	6 V
3 V analog supply voltage (AVDD3) to GND	5 V
3 V digital supply voltage (DVDD3) to GND	5 V
AINP, AINN to GND (voltage difference between pin and ground)	0.5 V to 4.5 V 3/
AINP to AINN (voltage difference between pins, common mode at AVDD5/2): 3/	
Short duration	-0.3 V to (AVDD5 + 0.3 V)
Continuous AC signal	1.25 V to 3.75 V
Continuous DC signal	1.75 V to 3.25 V
CLKINP, CLKINN to GND (voltage difference between pin and ground)	0.5 V to 4.5 V 3/
CLKINP to CLKINN (voltage difference between pins, common mode at AVDD5/2): 3/	
Continuous AC signal	1.1 V to 3.9 V
Continuous DC signal	2 V to 3 V
RESETP, RESETN to GND (voltage difference between pin to ground)	-0.3 V to (AVDD5 + 0.3 V) 3/
RESETP to RESETN (voltage difference between pins): 3/	
Continuous AC signal	1.1 V to 3.9 V
Continuous DC signal	2 V to 3 V
Data/OVR outputs to GND (voltage difference between pin and ground)	-0.3 V to (DVDD3 + 0.3 V) 3/
SDENB, SDIO, SCLK to GND (voltage difference between pin and ground)	-0.3 V to (AVDD3 + 0.3 V) 3/
ENA1BUS, ENPWD, ENEXTREF to GND (voltage difference between pin and ground)	-0.3 V to (AVDD5 + 0.3 V) 3/
Maximum junction temperature (T_J)	150°C
Storage temperature range	-65°C to +150°C
Electrostatic discharge (ESD) rating:	
Human body model (HDM)	2 kV
Thermal resistance, junction-to-case (θ_{JC})	0.849°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	21.81°C/W

1.4 Recommended operating conditions.

Supply voltage:	
AVDD5 to GND	4.75 V to 5.25 V
AVDD3 to GND	3.135 V to 3.465 V
DVDD3 to GND	3.135 V to 3.465 V
Analog input:	
Full scale differential input range	1.52 V_{PP} to 2 V_{PP}
Digital output:	
Differential output load	5 pF
Clock (CLK) input:	
CLK input sample rate (sine wave)	100 MSPS to 1000 MSPS
Clock amplitude, differential	0.6 V_{PP} to 1.5 V_{PP}
Clock duty cycle	45% to 55%
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ This package has built in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low impedance ground path, a thermal land is required on the surface of the printed circuit board (PCB) directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. The manufacturer recommends an 11.9 mm^2 board mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically at ground potential.

3/ Valid when supplies are within recommended operating range.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Analog inputs section							
Full scale differential input range		Programmable	1, 2, 3	01	1.52	2	V_{PP}
Reference voltage	V_{REF}		1, 2, 3	01	1.98	2.02	V
Dynamic accuracy section							
Resolution		No missing codes	4, 5, 6	01	12		Bits
Differential linearity error	DNL	f_{IN} = 125 MHz	4, 5, 6	01	-1	2.5	LSB
Integral non- linearity error	INL	f_{IN} = 125 MHz	4, 5, 6	01	-4.5	4.5	LSB
Offset error voltage		Default is trimmed near 0 mV	1, 2, 3	01	-2.5	2.5	mV
Power supply section 2/							
5 V analog supply current (Bus A and B active)	I_{AVDD5}	f_{IN} = 125 MHz, f_S = 1 GSPS	1, 2, 3	01		245	mA
5 V analog supply current (Bus A active)	I_{AVDD5}	f_{IN} = 125 MHz, f_S = 1 GSPS	1, 2, 3	01		255	mA
3.3 V analog supply current (Bus A and B active)	I_{AVDD3}	f_{IN} = 125 MHz, f_S = 1 GSPS	1, 2, 3	01		234	mA
3.3 V analog supply current (Bus A active)	I_{AVDD3}	f_{IN} = 125 MHz, f_S = 1 GSPS	1, 2, 3	01		242	mA
3.3 V digital supply current (Bus A and B active)	I_{DVDD3}	f_{IN} = 125 MHz, f_S = 1 GSPS	1, 2, 3	01		154	mA
3.3 V digital supply current (Bus A active)	I_{DVDD3}	f_{IN} = 125 MHz, f_S = 1 GSPS	1, 2, 3	01		85	mA
Total power dissipation (Bus A and B active)			1, 2, 3	01		2.5	W
Total power dissipation (Bus A active)			1, 2, 3	01		2.3	W
Total power dissipation		ENPWD = logic high (sleep enabled)	1, 2, 3	01		50	mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamics ac characteristics section							
Signal to noise ratio	SNR	f_{IN} = 125 MHz	4, 5, 6	01	54		dBFS
		f_{IN} = 600 MHz			53.5		
		f_{IN} = 850 MHz			53		
Spurious free dynamic range	SFDR	f_{IN} = 125 MHz	4, 5, 6	01	62		dBc
		f_{IN} = 600 MHz			60		
		f_{IN} = 850 MHz			56		
Second harmonic	HD2	f_{IN} = 125 MHz	4, 5, 6	01	62		dBc
		f_{IN} = 600 MHz			60		
		f_{IN} = 850 MHz			56		
Third harmonic	HD3	f_{IN} = 125 MHz	4, 5, 6	01	62		dBc
		f_{IN} = 600 MHz			60		
		f_{IN} = 850 MHz			56		
Worst harmonic/spur (other than HD2 and HD3)		f_{IN} = 125 MHz	4, 5, 6	01	62		dBc
		f_{IN} = 600 MHz			60		
		f_{IN} = 850 MHz			56		
Total harmonic distortion	THD	f_{IN} = 125 MHz	4, 5, 6	01	60		dBc
		f_{IN} = 600 MHz			58		
		f_{IN} = 850 MHz			55		
Signal to noise and distortion	SINAD	f_{IN} = 125 MHz	4, 5, 6	01	53		dBFS
		f_{IN} = 600 MHz			52.4		
		f_{IN} = 850 MHz			50.8		
Effective number of bits (using SINAD in dBFS)	ENOB	f_{IN} = 125 MHz	4, 5, 6	01	8.52		Bits
		f_{IN} = 600 MHz			8.42		
		f_{IN} = 850 MHz			8.16		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switching characteristics							
LVDS digital outputs	(DATA, OVR/SYNCOUT, CLKOUT)						
Differential output voltage(±)	V_{OD}	Terminated 100Ω differential	1, 2, 3	01	247	454	mV
Common mode output voltage	V_{OC}	Terminated 100Ω differential	1, 2, 3	01	1.125	1.375	V
LVDS digital inputs (RESET)							
Differential input voltage(±)	V_{ID}	Each input pin	1, 2, 3	01	175		mV
Common mode input voltage	V_{IC}	Each input pin	1, 2, 3	01	0.1	2.4	V
Digital inputs (SCLK, SDIO, SDENB)							
High level input voltage	V_{IH}		1, 2, 3	01	2	AVDD3 + 0.3	V
Low level input voltage	V_{IL}		1, 2, 3	01	0	0.8 V	V
Digital inputs (ENEXTREF, ENPWD, ENA1BUS)							
High level input voltage	V_{IH}		1, 2, 3	01	2	AVDD5 + 0.3	V
Low level input voltage	V_{IL}		1, 2, 3	01	0	0.8 V	V
Digital outputs (SDIO, SDO)							
High level output voltage	V_{OH}	I_{OH} = 250 μA	1, 2, 3	01	2.8		V
Low level output voltage	V_{OL}	I_{OL} = 250 μA	1, 2, 3	01		0.4	V
Clock inputs							
Differential input resistance	R_{IN}	CLKINP, CLKINN	4, 5, 6	01	100	190	Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LVDS output timing (DATA, CLKOUT, OVR/SYNCOUT) 4/							
Clock period	t_{CLK}		9, 10, 11	01	1	10	ns
Clock pulse duration, high	t_{CLKH}	Assuming worst case 45/55 duty cycle	9, 10, 11	01	0.45		ns
Clock pulse duration, low	t_{CLKL}	Assuming worst case 45/55 duty cycle	9, 10, 11	01	0.45		ns
Setup time, single bus mode 5/, 6/	t_{SU-SBM}	Data valid to CLKOUT edge, 50% CKLIN duty cycle	9, 10, 11	01	290		ps
Hold time, single bus mode 6/	t_{H-SBM}	CLKOUT edge to data invalid, 50% CLKIN duty cycle	9, 10, 11	01	410		ps
Setup time, dual bus mode 6/	t_{SU-DBM}	Data valid to CLKOUT edge, 50% CKLIN duty cycle	9, 10, 11	01	550		ps
Hold time, dual bus mode 6/	t_{H-DBM}	CLKOUT edge to data invalid, 50% CLKIN duty cycle	9, 10, 11	01	1150		ps
LVDS input timing (RESETIN)							
RESET setup time 6/	t_{RSU}	RESETP going high to CLKINP going low	9, 10, 11	01	325		ps
RESET hold time 6/	t_{RH}	CLKINP going low to RESETP going low	9, 10, 11	01	325		ps
Serial interface timing							
Setup time, serial enable	$t_{S-SDENB}$	SDENB falling to SCLK rising	9, 10, 11	01	20		ns
Hold time, serial enable	$t_{H-SDENB}$	SCLK falling to SENDB rising	9, 10, 11	01	25		ns
Setup time, SDIO	t_{S-SDIO}	SDIO valid to SCLK rising	9, 10, 11	01	10		ns
Hold time, SDIO	t_{H-SDIO}	SCLK rising to SDIO transition	9, 10, 11	01	10		ns
Frequency	f_{SCLK}		9, 10, 11	01		10	MHz
SCLK period	t_{SCLK}		9, 10, 11	01	100		ns
Minimum SCLK high time	t_{SCLKH}		9, 10, 11	01	40		ns
Minimum SCLK low time	t_{SCLKL}		9, 10, 11	01	40		ns
Data output delay	t_{DDATA}	Data output (SDO/SDIO) delay after SCLK falling, 10 pF load	9, 10, 11	01	75		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Interleaving adjustments							
Offset adjustments							
Resolution			4, 5, 6	01	9		Bits
Differential linearity error	DNL		4, 5, 6	01	-2.5	2.5	LSB
Integral non-linearity error	INL		4, 5, 6	01	-3	3	LSB
Gain adjustments							
Resolution			4, 5, 6	01	12		Bits
Differential linearity error	DNL		4, 5, 6	01	-4	4	LSB
Integral non-linearity error	INL		4, 5, 6	01	-8	8	LSB
Input clock fine phase adjustment							
Resolution			4, 5, 6	01	6		Bits
Differential linearity error	DNL		4, 5, 6	01	-2	2.5	LSB
Integral non-linearity error	INL		4, 5, 6	01	-2.5	4	LSB
Input clock coarse phase adjustment.							
Resolution			4, 5, 6	01	5		Bits
Differential linearity error	DNL		4, 5, 6	01	-1	1	LSB
Integral non-linearity error	INL		4, 5, 6	01	-1	5	LSB
Functional test		See 4.4.1b	7, 8	01			

1/ Unless otherwise specified, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, -1 dBFS differential input, and 1.5 V_{PP} differential clock.
2/ All power values assume LVDS output current is set to 3.5 mA.
3/ Unless otherwise specified, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5 V_{PP} differential clock.
4/ LVDS output timing measured with a differential 100Ω load placed ~ 4 inches from the device. Measured differential load capacitance is 3.5 pF. Measured probes and other parasites add ~ 1 pF. Total approximate capacitive load is 4.5 pF differential. All timing parameters are relative to the device pins, with the loading as stated.
5/ In single bus mode at 1 GSPS (1 ns clock), the minimum output setup/hold times over process and temperature provide a minimum 700 ps of data valid window, with 300 ps of uncertainly.
6/ This parameter is specified by design or characterization, but not production tested. Bench data used for limit verification, the tests require pico second resolution which is not possible in ATE setup.

Case X

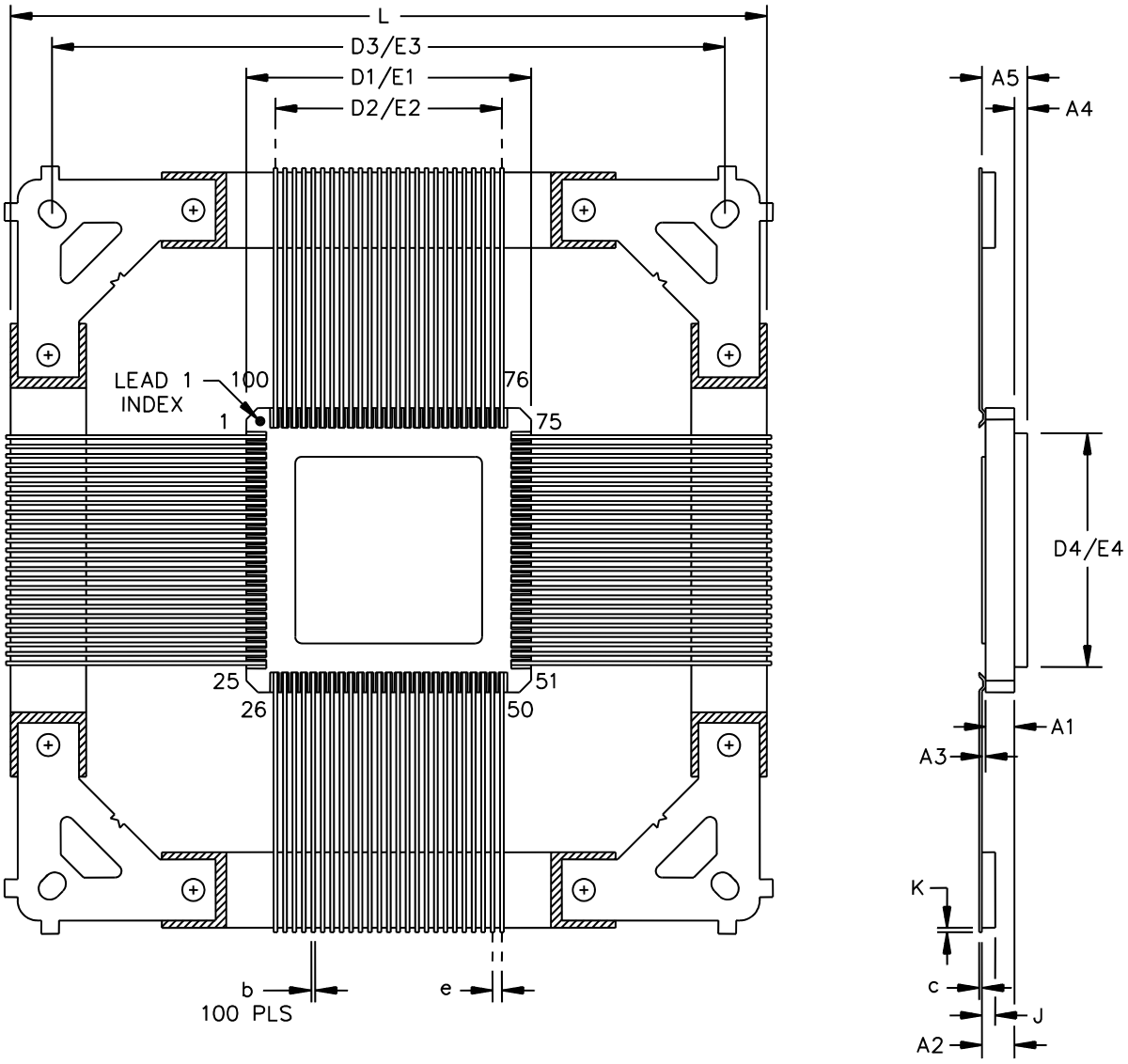


FIGURE 1. Case outline.

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.080	NOM	2.03	NOM
A2	---	0.105	---	2.67
A3	0.002	0.014	0.05	0.36
A4	0.030	NOM	0.762	NOM
A5	---	0.124	---	3.150
b	0.010	0.006	0.15	0.25
c	0.004	0.008	0.10	0.20
D1/E1	0.742	0.758	18.850	19.250
D2/E2	0.600	BSC	15.240	BSC
D3/E3	1.800	BSC	45.720	BSC
D4/E4	0.624	0.636	15.842	16.162
e	0.025	BSC	0.635	BSC
J	---	0.036	---	0.90
K	---	0.020	---	0.51
L	1.980	2.020	50.300	51.300
n	100			

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated and can be solder dipped.
5. All leads are not shown for clarity purposes.
6. Lid and heat sink are connected to GND leads

FIGURE 1. Case outline - continued.

Device type	01			
Case outline	X			
Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	AVDD5		26	CLKOUTBN
2	AVDD3		27	CLKOUTBP
3	AGND		28	DB5N
4	CLKINP		29	DB5P
5	CLKINN		30	DB4N
6	AGND		31	DB4P
7	AVDD3		32	DB3N
8	AGND		33	DB3P
9	AVDD3		34	DB2N
10	RESETN		35	DB2P
11	RESETP		36	DB1N
12	DB11N		37	DB1P
13	DB11P		38	DVDD3
14	DB10N		39	DGND
15	DB10P		40	DB0N
16	DB9N		41	DB0P
17	DB9P		42	OVRBN
18	DB8N		43	OVRBP
19	DB8P		44	OVRAN
20	DB7N		45	OVRAP
21	DB7P		46	DA0N
22	DB6N		47	DA0P
23	DB6P		48	DA1N
24	DVDD3		49	DA1P
25	DGND		50	DVDD3

FIGURE 2. Terminal connections.

Device type	01			
Case outline	X			
Terminal number	Terminal symbol		Terminal number	Terminal symbol
51	DGND		76	AVDD5
52	DA2N		77	SDENB
53	DA2P		78	SCLK
54	DA3N		79	SDIO
55	DA3P		80	SDO
56	DA4N		81	ENA1BUS
57	DA4P		82	ENPWD
58	DA5N		83	ENEXTREF
59	DA5P		84	AGND
60	CLKOUTAN		85	AVDD3
61	CLKOUTAP		86	AVDD5
62	DA6N		87	VREF
63	DA6P		88	AGND
64	DVDD3		89	VCM
65	DGND		90	AVDD5
66	DA7N		91	AGND
67	DA7P		92	AVDD5
68	DA8N		93	AGND
69	DA8P		94	AINP
70	DA9N		95	AINN
71	DA9P		96	AGND
72	DA10N		97	AVDD5
73	DA10P		98	AGND
74	DA11N		99	AVDD5
75	DA11P		100	AGND

FIGURE 2. Terminal connections - continued.

Terminal symbol	Description
AINP, AINN	Analog differential input signal (positive, negative). Includes 100 Ω differential load on chip.
AVDD5	Analog power supply (5 V).
AVDD3	Analog power supply (3.3 V).
DVDD3	Output driver power supply (3.3 V).
AGND	Analog ground.
DGND	Digital ground.
CLKINP, CLKINN	Differential input clock (positive, negative). Includes 160 Ω differential load on chip.
DA0N, DAOP	Bus A, LVDS digital output pair, least significant bit (LSB) (P = positive output, N = negative output).
DA1N - DA10N, DA1P - DA10P	Bus A, LVDS digital output pairs (bits 1 - 10).
DA11N, DA11P	Bus A, LVDS digital output pair, most significant bit (MSB).
CLKOUTAN, CLKOUTAP	Bus A, clock output (data ready), LVDS output pair.
DB0N, DB0P	Bus B, LVDS digital output pair, least significant bit (LSB) (P = positive output, N = negative output).
DB1N - DB10N, DB1P - DB10P	Bus B, LVDS digital output pairs (bits 1 - 10).
DB11N, DB11P	Bus B, LVDS digital output pair , most significant bit (MSB).
CLKOUTBN,CLKOUTBP	Bus B, clock output (data ready), LVDS output pair
OVRAN, OVRAP	Bus A, overrange indicator LVDS output. A logic high signals an analog input in excess of the full scale range. Becomes SYNCOUTA when SYNC mode is enabled in register 0x05.
OVRBN, OVRBP	Bus B, overrange indicator LVDS output. A logic high signals an analog input in excess of the full scale range. Becomes SYNCOUTB when SYNC mode is enabled in register 0x05.
RESETN, RESETP	Digital reset input. LVDS input pair. Inactive if logic low. When clocked in a high state, this is used for resetting the polarity of CLKOUT signal pair(s). If SYNC mode is enabled in register 0x05, this input also provides a SYNC item stamp with the data sample present when RESET is clocked by the ADC, as well as CLKOUT polarity reset. Includes 100 Ω differential load on chip.
SCLK	Serial interface clock.
SDIO	Bi-directional serial interface data in 3 pin mode (default) for programming/reading internal registers. In 4 pin interface mode (register 0x01), the SDIO pin is an input only.
SDO	Uni-directional serial interface data in 4 pin mode (register 0x01) provides internal register settings. The SDO pin is in high impedance state in 3 pin interface mode (default)
SDENB	Active low serial data enable, always an input. Use to enable the serial interface. Internal 100 kΩ pull up resistor.

FIGURE 2. Terminal connections - continued.

Terminal symbol	Description
VREF	Reference voltage input (2 V nominal). A 0.1 μF capacitor to AGND is recommended, but not required.
ENA1BUS (SEE NOTE 1)	Enable single output bus mode (2 bus mode is default), active high. This pin is logic OR'd with address 0x02h bit <0>.
ENPWD (SEE NOTE 1)	Enable powerdown, active high. Places the converter into power saving sleep mode when high. This pin is logic OR'd with address 0x05h bit <6>.
ENEXTREF (SEE NOTE 1)	Enable external reference mode, active high. Device uses an external voltage reference when high. This pin is logic OR'd with address 0x05h bit <2>.
VCM	Analog input common mode voltage, output (for dc coupled applications, nominally 2.5 V). A 0.1 μF capacitor to AGND is recommended, but not required.

NOTE: 1. This pin contains an internal ~ 40 kΩ pull down resistor, to ground.

FIGURE 2. Terminal connections - continued.

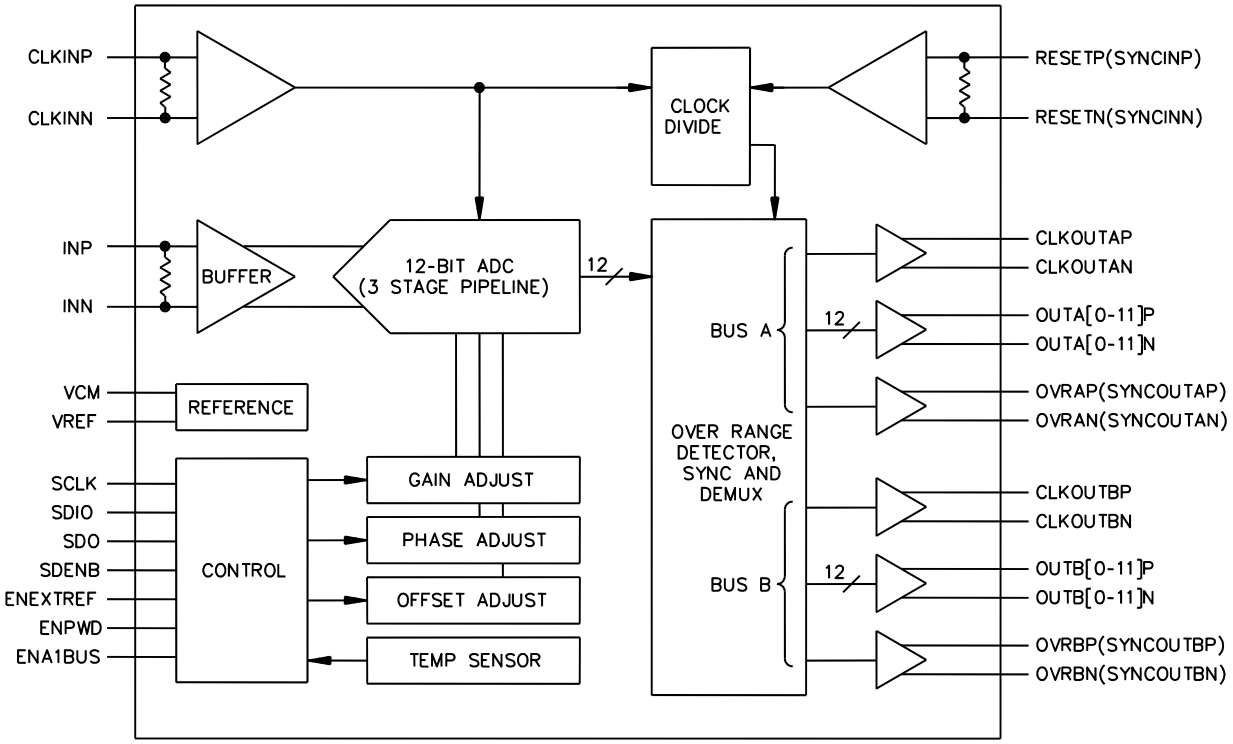
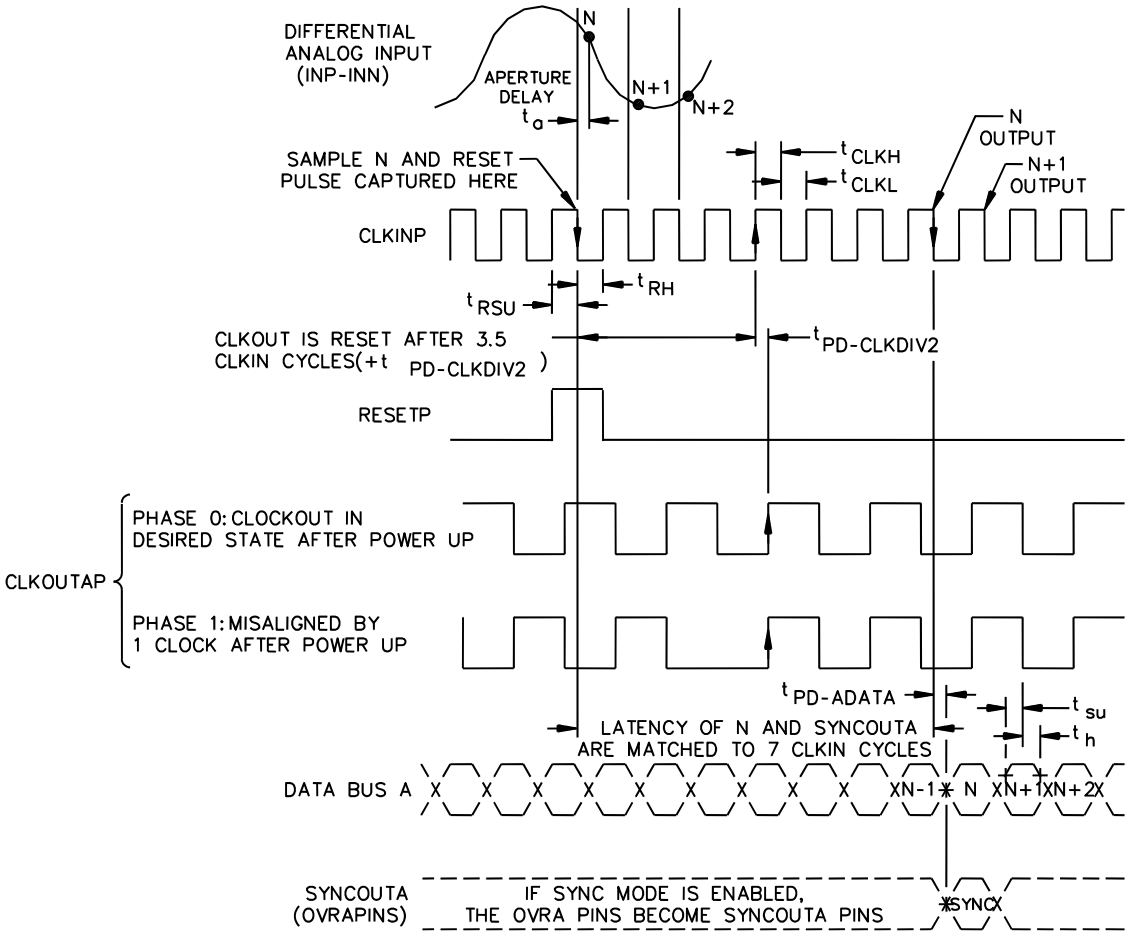


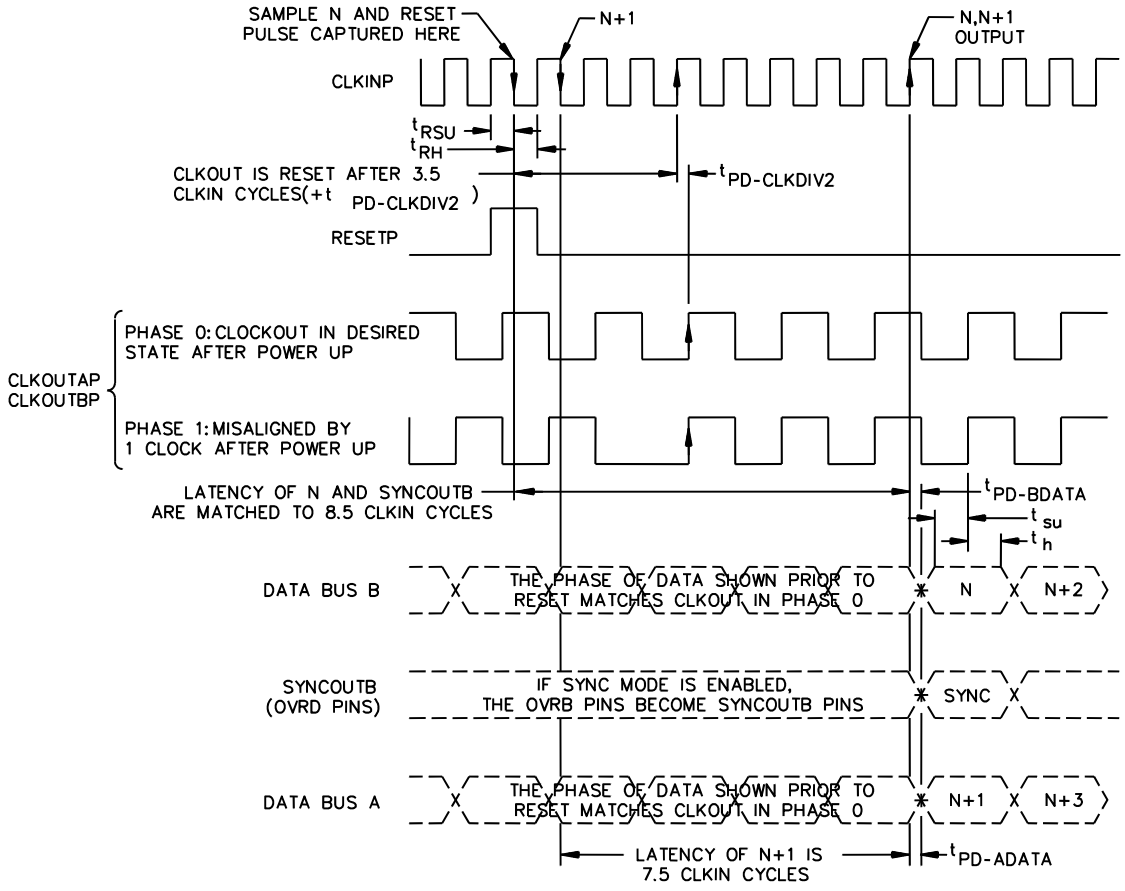
FIGURE 3. Block diagram.



Single Bus Mode

NOTE: Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/2, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTA transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit. Bus B is not active in single bus mode.

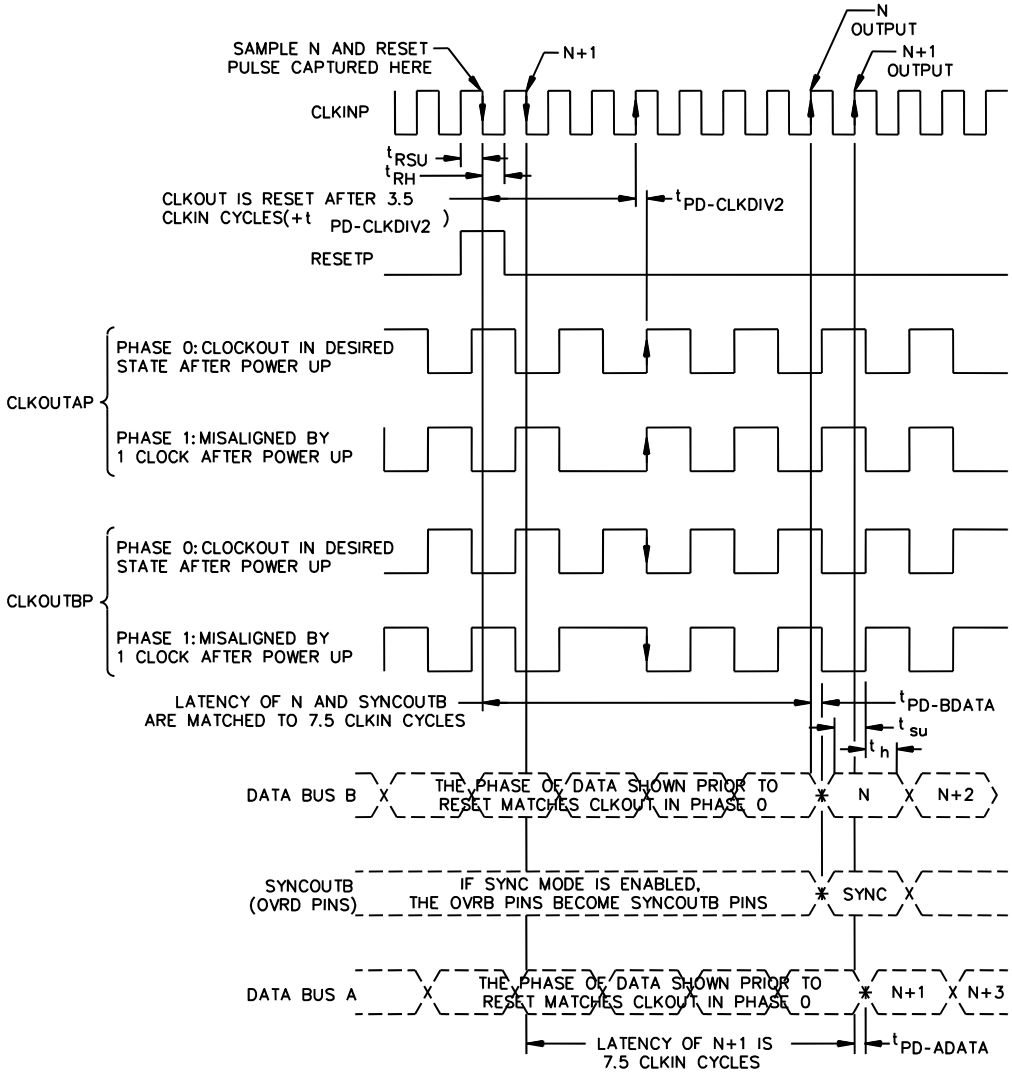
FIGURE 4. Timing waveforms.



Dual Bus Mode – Aligned, CLKOUT Divide By 2

NOTE: Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/2, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

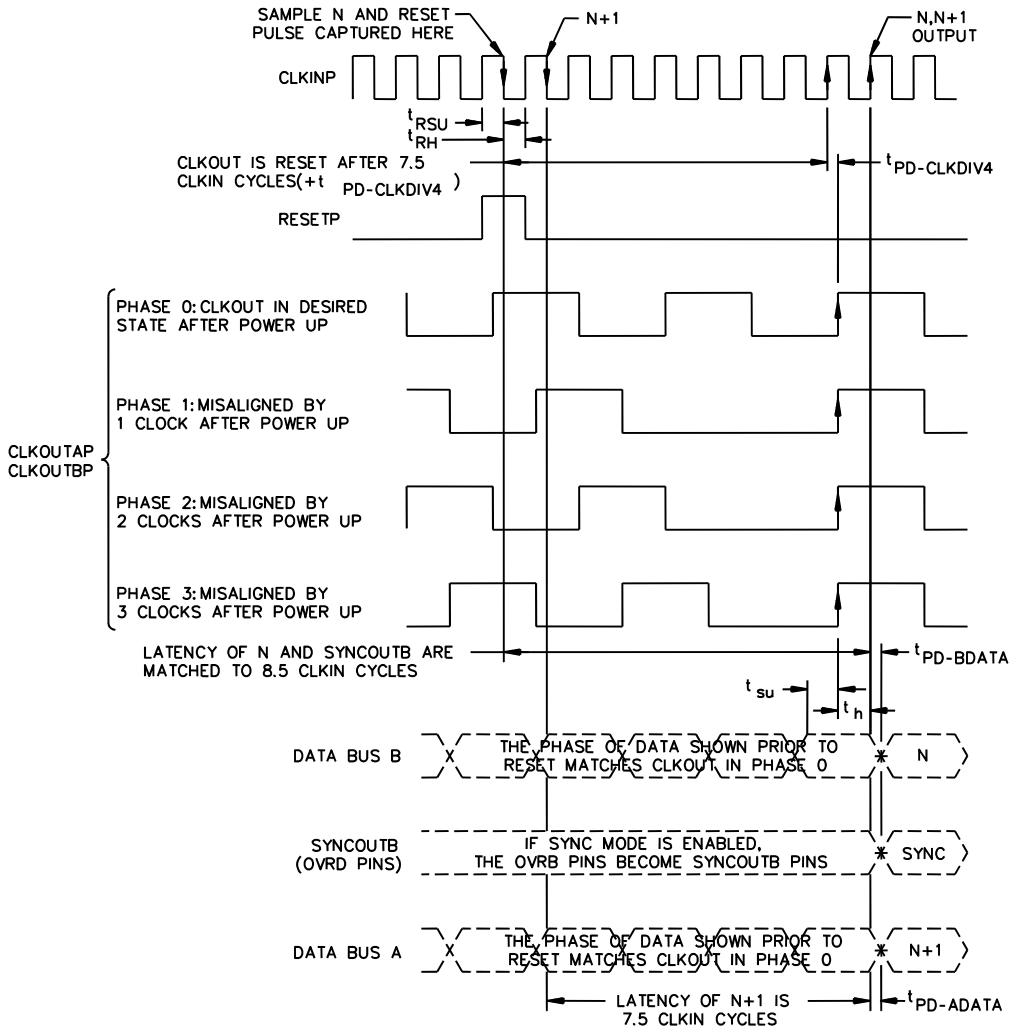
FIGURE 4. Timing waveforms - continued.



Dual Bus Mode – Staggered, CLKOUT Divide By 2

NOTE: Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/2, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

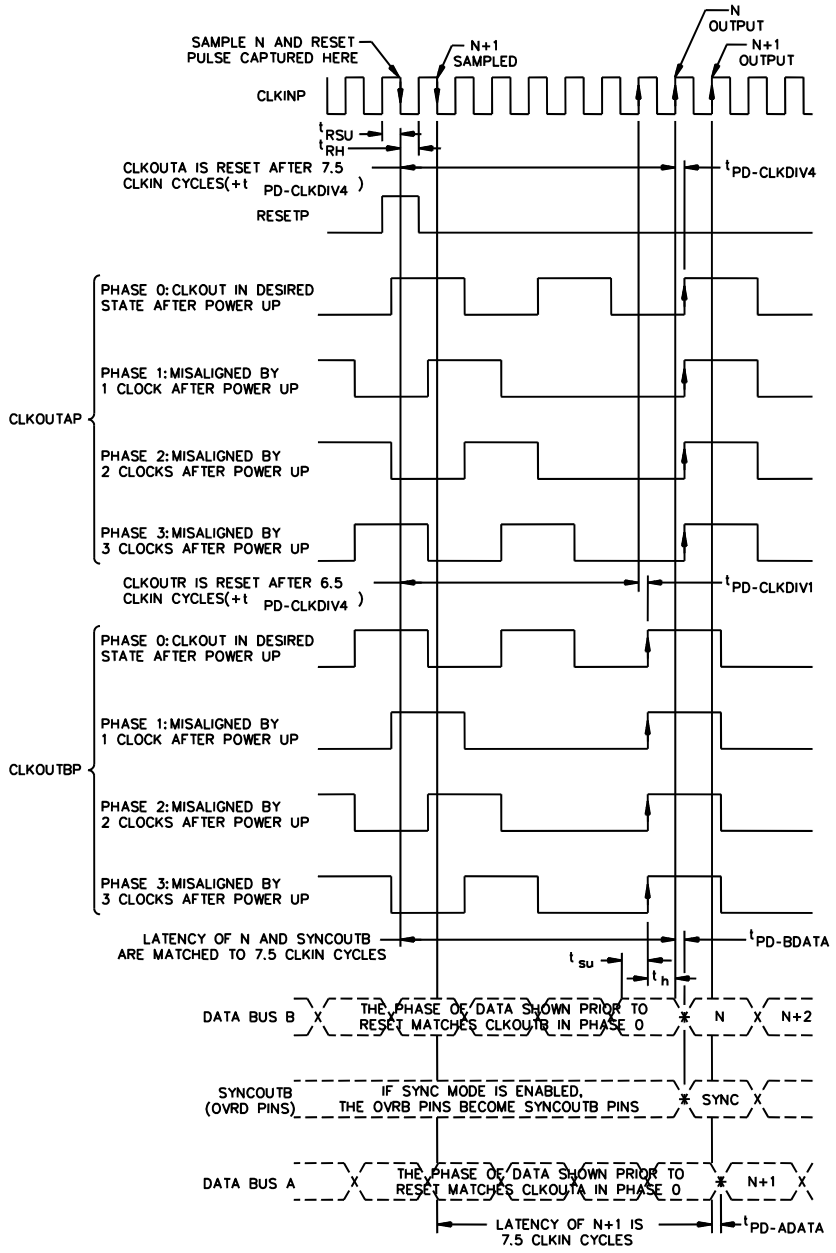
FIGURE 4. Timing waveforms - continued.



Dual Bus Mode – Aligned, CLKOUT Divide By 4

NOTE: Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/4, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

FIGURE 4. Timing waveforms - continued.



Dual Bus Mode – Staggered, CLKOUT Divide By 4

NOTE: Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/4, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

FIGURE 4. Timing waveforms - continued.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 4	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 2/
Group D end-point electrical parameters (see 4.4)	1, 4	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Operating life test delta parameters. T_C = +25°C.

Parameters	Symbol	Condition	Delta limits
5 V analog supply current (Bus A and B active)	I_{AVDD5}	f_{IN} = 125 MHz, f_S = 1 GSPS	±5 mA
3.3 V analog supply current (Bus A and B active)	I_{AVDD3}	f_{IN} = 125 MHz, f_S = 1 GSPS	±5 mA
3.3 V digital supply current (Bus A and B active)	I_{DVDD3}	f_{IN} = 125 MHz, f_S = 1 GSPS	±5 mA
Reference voltage	V_{REF}		±10 mV

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-05-20

Approved sources of supply for SMD 5962-09240 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0924001VXC	01295	ADS5400MHFSV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243